(FOR REFERENCE ONLY, NOT RECOMMENDED FOR NEW DESIGNS)

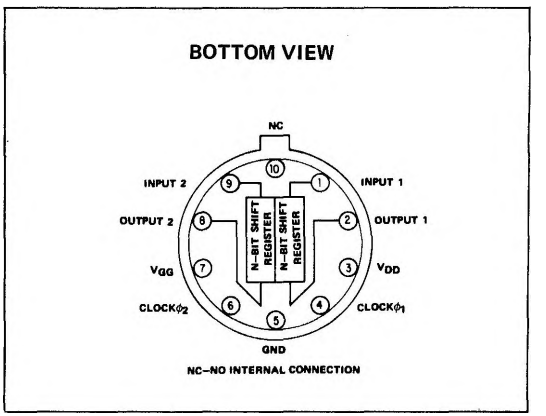
METAL GATE MOS 2000 SERIES

DESCRIPTION

The S2001K, S2002K, S2003K, S2004K, and S2005K are Dual Static Shift Registers manufactured with a "P" channel enhancement mode process.

The registers vary in length from dual 16 to dual 100. Two power supplies and 2 external 28 volt clocks are required. Static operation is assured with a third clock phase that is generated on the chip. The pin configuration allows interchanging of register lengths without rewiring the socket. Data is transferred into the register during ϕ_1 and output data appears on the negative-going edge of ϕ_2. For static operation ϕ_1 must be a "0" and ϕ_2 "1".

PIN CONFIGURATION



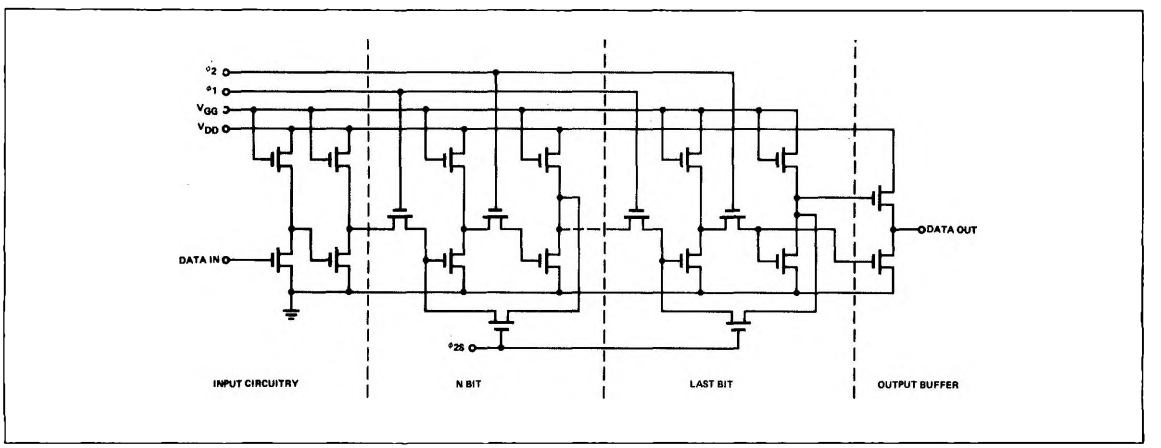
PARTS IDENTIFICATION TABLE

PART NO.	BIT LENGTH	PACKAGE
S2001K	16	10 Pin TO-100
S2002K	25	10 Pin TO-100
S2003K	32	10 Pin TO-100
S2004K	50	10 Pin TO-100
S2005K	100	10 Pin TO-100

ABSOLUTE MAXIMUM RATINGS

V_{dd} with respect to Gnd	-16V to 0.3V
V_{gg} with respect to Gnd	-30V to 0.3V
Clock and In with respect to Gnd	-30V to 0.3V
Operating Temperature	-55°C to +85°C
Storage Temperature	-55°C to +150°C

CIRCUIT SCHEMATIC



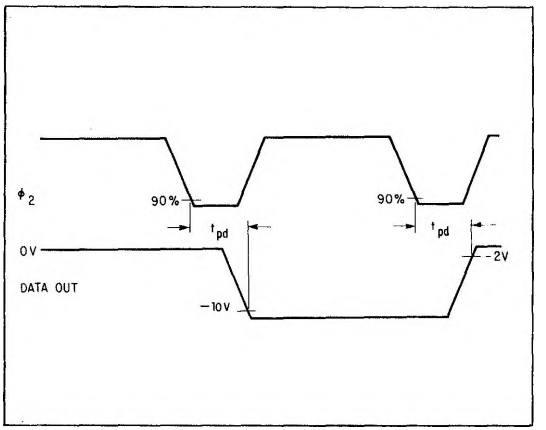
ELECTRICAL CHARACTERISTICS (Notes: 1, 2, 3, 4 and 5)

CHARACTERISTICS	LIMITS				TEST CONDITIONS							NOTES
	MIN	TYP	MAX	UNITS	TEMP °C	V_{DD}	V_{GG}	Vin	$V\phi_1$	$V\phi_2$	OUTPUT	
"1" Output Voltage	-11	-13		V		-13	-27	-10	-27	-27		5
"0" Output Voltage		-0.3	-1	V		-15	-29	-2	-29	-29		5
Output Drive Capability												
2001	-8	-10		V		-13	-27	-10	-27	-27		R_L = 17kΩ to Gnd
	-4	-6		V		-13	-27	-10	-27	-27		R_L = 4 kΩ to Gnd
2002/3/4/5	-10	-11		V		-13	-27	-10	-27	-27		R_L = 17 kΩ to Gnd
	-6	-8		V		-13	-27	-10	-27	-27		R_L = 4 kΩ to Gnd
Input Leakage Current												
Data Inputs			0.5	μA	+85	0	0	-20	0	0		
Clock Inputs												
ϕ_1			50	μA	+85	0	0	0	-28	0		
ϕ_2			50	μA	+85	0	0	0	0	-28		
Output Impedance												
2001			2.5	kΩ		-13	-27	-2	-27	-27	0 to -1V	
2002/3/4/5			1.5	kΩ		-13	-27	-2	-27	-27	0 to -1V	
Input Capacitance												
Data Inputs		3	5	pF	25	-14	-28	0	0	0		8
Clock Inputs												
2001		8	10	pF	25	-14	-28	0	0	0		8
2002		8	12	pF	25	-14	-28	0	0	0		8
2003		8	13	pF	25	-14	-28	0	0	0		8
2004		12	18	pF	25	-14	-28	0	0	0		8
2005		16	33	pF	25	-14	-28	0	0	0		8
Power Supply Current												
I_{DD}												
2001		-3	-10	mA	-55	-15	-29		0	-29		
2002		-5	-20	mA	-55	-15	-29		0	-29		
2003		-6	-24	mA	-55	-15	-29		0	-29		
2004		-7	-17	mA	-55	-15	-29		0	-29		
2005		-14	-32	mA	-55	-15	-29		0	-29		
I_{GG}												
2001/2/3		-0.8	-3.5	mA	-55	-15	-29		0	-29		
2004/5		-0.5	-3.0	mA	-55	-15	-29		0	-29		
Propagation Delay (tpd) from ϕ_2												
2001		300	475	ns	25	-14	-28		-28	-28		6, 7
2002/3/4/5		300	450	ns	25	-14	-28		-28	-28		6, 7

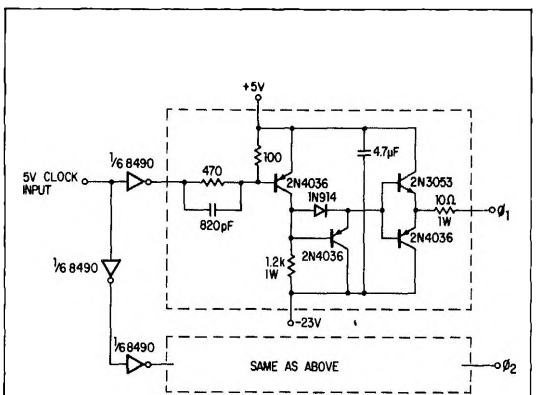
NOTES FOR ELECTRICAL CHARACTERISTICS:

1. Parameter valid over operating temperature range unless otherwise specified.
2. All voltage measurements are referenced to the ground terminal. Terminals not specifically referenced are tied to ground.
3. Negative logic definition: "DOWN" Level = "1", "UP" Level = "0".
4. Manufacturer reserves the right to make design and process changes and improvements.
5. Output voltage levels valid from D.C. to 1 MHz.
6. See output timing diagram.
7. Output load is 10 pF and 1 MΩ
8. f = 1 MHz, Vac = 25 mV_{rms}. All pins not specifically referenced are tied to guard terminal for capacitance tests. Output pins are left open.
9. All typical values are at 25°C and nominal supply voltages.

OUTPUT TIMING DIAGRAM



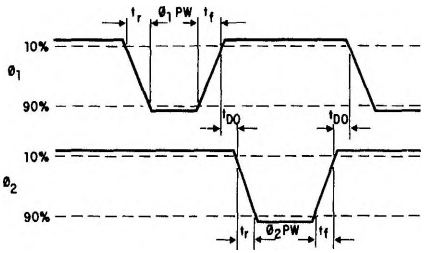
CLOCK DRIVER



Note: At high repetition rates and/or high capacitance loads, the transistors may require heat sinking, i.e., 1000 pF at 1 MHz.

FORCING FUNCTIONS

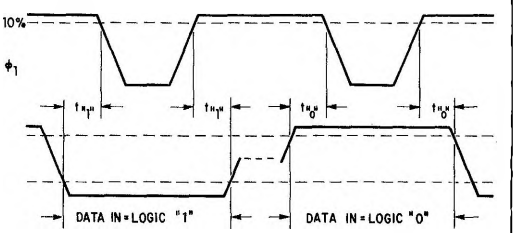
CLOCK REQUIREMENTS



VOLTAGE LEVELS	MIN	TYP	MAX	UNITS
ϕ_1 ϕ_2 "0"	0	-1	-2.0	Volts
ϕ_1 ϕ_2 "1"	-27	-28	-29	Volts
TIMING				
t_r & t_f	.025		5	μsec
ϕ_1 PW	0.4		10	μsec
ϕ_2 PW	0.4			μsec
t_{DO}	0			μsec

Note: ϕ_2 may not be at "0" logic level for more than 10 μs.

INPUT REQUIREMENTS



CHARACTERISTIC	MIN	MAX	UNITS
Data in "0"	+0.3	-2.0	Volts
Data in "1"	-10		Volts
$t_{"1"}$ & $t_{"0"}$	0		μsec

Note: Data In must be stable between the 10% points of ϕ_1.