(FOR REFERENCE ONLY, NOT RECOMMENDED FOR NEW DESIGNS)

METAL GATE MOS 2000 SERIES

DESCRIPTION

The N2010K Dual 100-Bit Static Shift Register is designed for use at shift rates from 0 to 3 MHz.* The device employs "P" channel enhancement mode MOS techniques. Power supply requirements are -14 and -28 Vdc. Clocking is provided by two external -28 volt clock phases. A delayed second clock phase (ϕ_{2S}) is generated on the chip.

Data is transferred into the register during ϕ_1. Output data appears on the negative going edge of ϕ_2. For static operation, ϕ_1 must be a "0" and ϕ_2 a "1".

The N2010K is a direct pin replacement for the S2005K/ 3003 1MHz Static Shift Register.

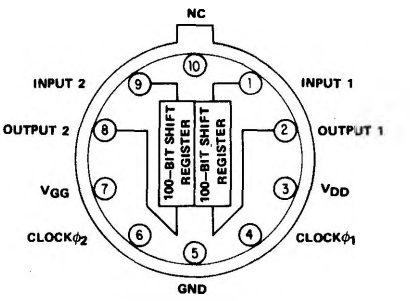
*(25°)

ABSOLUTE MAXIMUM RATINGS:

V_{DD} with respect to Gnd	-16V to 0.3V
V_{GG} with respect to Gnd	-30 to 0.3V
Clock and Input with respect to Gnd	-30V to 0.3V
Operating Temperature	0°C to +70°C
Storage Temperature	-55°C to +150°C

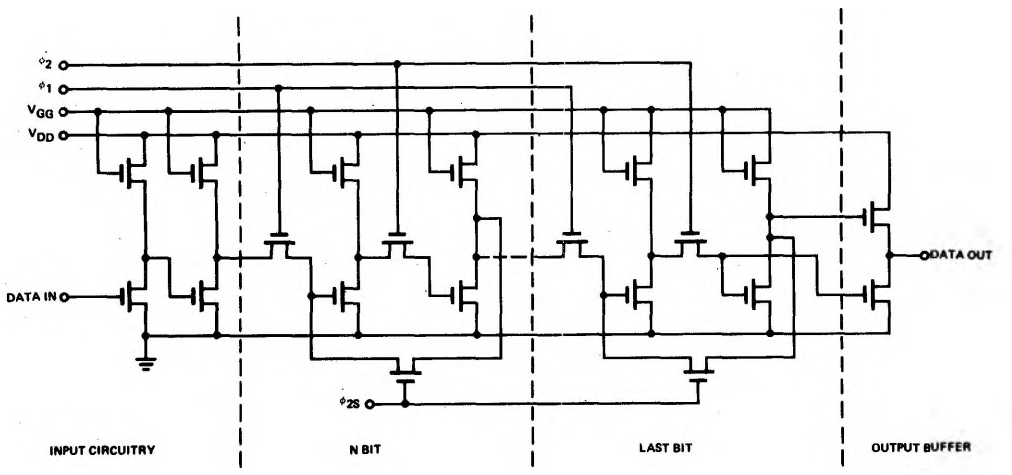
PIN CONFIGURATION

BOTTOM VIEW



NC–NO INTERNAL CONNECTION

CIRCUIT SCHEMATIC



ELECTRICAL CHARACTERISTICS (Notes: 1, 2, 3, 4, 9)

RECOMMENDED POWER SUPPLY VOLTAGES: V_{DD} = −14 ±1 Vdc, V_{GG} = −28 ±1Vdc

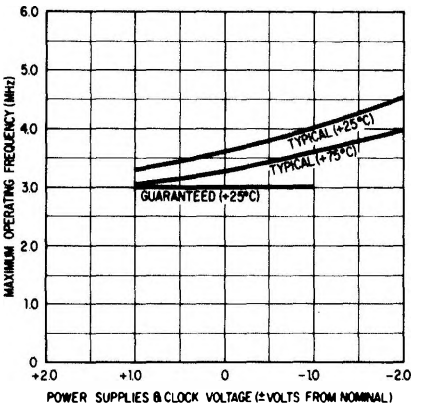
CHARACTERISTICS	LIMITS			UNITS	TEST CONDITIONS							NOTES
	MIN	TYP	MAX		TEMP °C	V_{DD}	V_{GG}	V_{in}	$V_{\phi1}$	$V_{\phi2}$	OUTPUT	
"1" Output Voltage	−8	−10		V	25	−13	−27	−7	−27	−27		5, 7
"0" Output Voltage		−0.3	−1.0	V	25	−15	−29	−2	−29	−29		5, 7
Output Drive Capability	−4	−6		V	25	−13	−27	−7	−27	−27		R_L = 4kΩ to Gnd
Input Leakage Current												
Data Inputs			−0.5	μA	25	0	0	−15	0	0		
Clock Inputs												
ϕ_1			−50	μA	25	0	0	0	−28	0		
ϕ_2			−50	μA	25	0	0	0	0	−28		
Output Impedance			1.5	kΩ	25	−13	−27	−2	−27	−27	0 to −1V	
Input Capacitance												
Data Inputs		3	5	pF	25	−14	−28	0	0	0		8
Clock Inputs		16	33	pF	25	−14	−28	0	0	0		8
Power Supply Current												
I_{DD}		−14	−20	mA	25	−15	−29		0	−29		
I_{GG}		−0.8	−3.0	mA	25	−15	−29		0	−29		
Propagation Delay (tdp) from ϕ_2		200	250	ns	25	−14	−28		−28	−28		6, 7

NOTES:

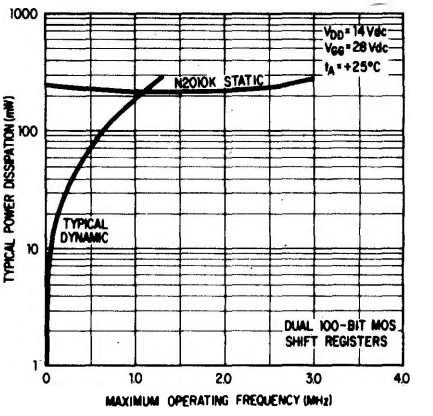
1. Parameter valid at +25°C unless otherwise specified
2. All voltage measurements are referenced to the ground terminal. Terminals not specifically referenced are tied to ground
3. Negative logic definition: "DOWN" Level = "1", "UP" Level = "0".
4. Manufacturer reserves the right to make design and process changes and improvements
5. Output voltage levels valid from DC to 3 MHz.
6. See output timing diagram.
7. Output load is 10pF and 1 MΩ
8. f = 1 MHz, Vac = 25mV rms. All pins not specifically referenced are tied to guard terminal for capacitance tests. Output pins are left open.
9. All typical values are at 25°C and nominal supply voltages

TYPICAL PERFORMANCE CHARACTERISTICS

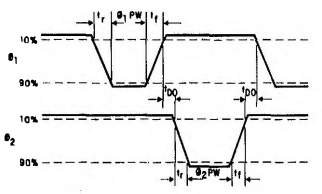
MAXIMUM OPERATION FREQUENCY
VERSUS CLOCK AND SUPPLY VOLTAGE



POWER DISSIPATION
VERSUS OPERATING FREQUENCY



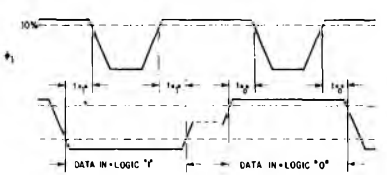
CLOCK REQUIREMENTS



VOLTAGE LEVELS	MIN	NOM	MAX	UNITS
ϕ_1 ϕ_2 "0"	0	-1	-2.0	Volts
ϕ_1 ϕ_2 "1"	-27	-28	-29	Volts
TIMING				
t_r & t_f	.010		5	μsec
ϕ_1 PW	0.10		10	μsec
ϕ_2 PW	0.15			μsec
t_{DO}	0			μsec
Clock Repetition Rate	0		3	MHz

Note: ϕ_2 may not be at "0" logic level for more than 10 μs.

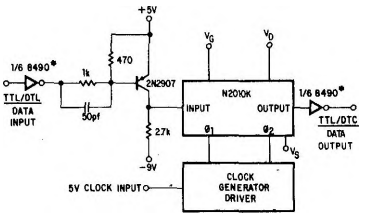
INPUT REQUIREMENTS



CHARACTERISTIC	MIN	MAX	UNITS
Data in "0"	+0.3	-2.0	Volts
Data in "1"	-7.0		Volts
$t_{"1"}$ & $t_{"0"}$	0		μsec

Note: Data In must be stable between the 10% points of ϕ_1.

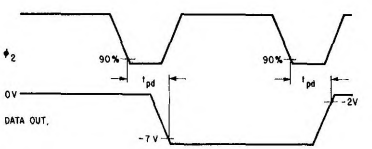
TTL INTERFACE REQUIREMENTS



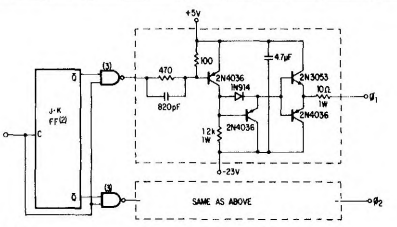
NOTES:

1. Register ground (V_S) is tied to the bipolar integrated circuit V_{CC} power supply for proper biasing.
2. V_S = +5VDC
   V_D = -9 VDC
   V_G = -23 VDC
3. *Signetics Corp. N8490A

OUTPUT TIMING DIAGRAM



CLOCK DRIVER



NOTES:

1. At high repetition rates and/or high capacitance loads, the transistors may require heat sinking, i.e., 1000 pF at 3MHz.
2. ½ N8822B, SP322B etc.
3. ½ N8880A, SP387A etc.