21F02-F,I,N • 21F02-2 - F,I,N • 21F02-4 - F,I,N

DESCRIPTION

The 21F02 is a high speed static random access memory element using n-channel MOS devices integrated on a monolithic array. It uses fully dc stable (static) circuitry and therefore requires no clocks or refreshing to operate. The data is read out nondestructively and has the same polarity as the input data.

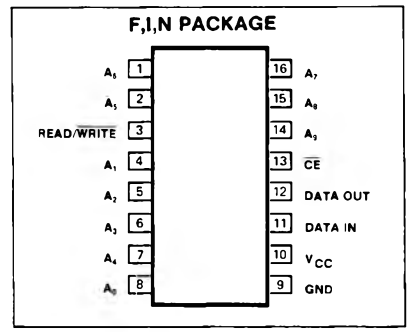
The 21F02 is designed for memory applications where high performance, low cost, large bit storage, and simple interfacing are important design objectives. A separate chip enable (CE) lead allows easy selection of an individual package when outputs are OR-tied.

The Signetics 21F02 is fabricated with n-channel silicon gate technology. This technology allows the design and production of high performance easy to use MOS circuits and provides a higher functional density on a monolithic chip than either conventional MOS technology or p-channel silicon gate technology.

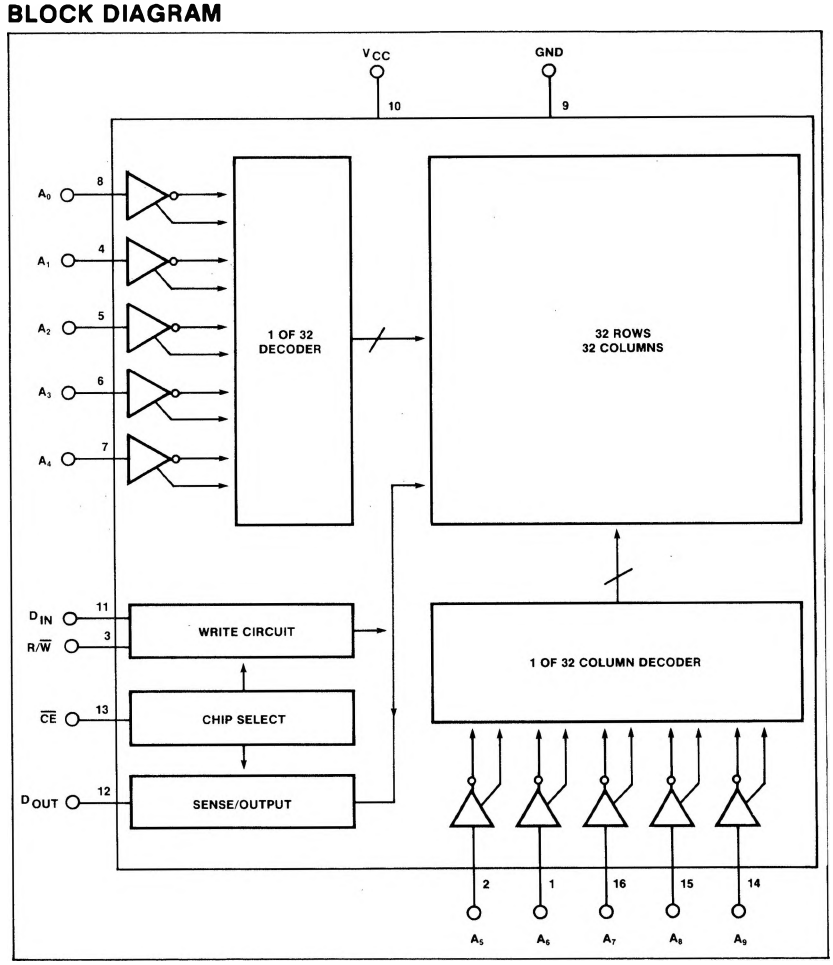
FEATURES

- **Fully TTL compatible**
- **Single 5V supply**

PIN CONFIGURATION



BLOCK DIAGRAM



ABSOLUTE MAXIMUM RATINGS[1]

	PARAMETER	RATING	UNIT
	Temperature range		°C
T_{STG}	Storage	-65 to 150	
P_D	Power dissipation[2]		
	N package	640	mW
	F package	1	W
	I package	1	W
	All input, output and supply voltages with respect to ground	-0.5 to 7	V

DC ELECTRICAL CHARACTERISTICS

T_A = 0°C to 70°C, V_{CC} = 5V ± 5% unless otherwise specified.

	PARAMETER	TEST CONDITIONS	LIMITS			UNIT
			Min	Typ[3]	Max	
	Input voltage					V
V_{IL}	Low		-0.5		0.8	
V_{IH}	High		2.0		V_{CC}	
	Output voltage					V
V_{OL}	Low	I_{OL} = 2.1mA			0.4	
V_{OH}	High	I_{OH} = -100μA	2.4			
I_{LI}	Input load current (All input pins)	V_{IN} = 0 to 5.25V			10	μA
	Output leakage current	$\overline{CE}$ = 2.0V				μA
I_{LOH}		V_{OUT} = 2.4 to V_{CC}			5	
I_{LOL}		V_{OUT} = 0.4V			-10	
	Supply current	All inputs = 5.25V, Data out open				mA
I_{CC1}		T_A = 25°C		30	60	
I_{CC2}		T_A = 0°C			70	

AC ELECTRICAL CHARACTERISTICS

T_A = 0°C to 70°C, V_{CC} = 5V ± 5% unless otherwise specified,
Input pulse levels = 0.65 to 2.2V, Input pulse rise and fall times = 20ns,
Timing measurement reference level = 1.5V,
Output load = 1 TTL gate and C_L = 100pF

	PARAMETER	TO	FROM	21F02			21F02-2			21F02-4			UNIT
				Min	Typ[3]	Max	Min	Typ[3]	Max	Min	Typ[3]	Max	
	READ CYCLE												
t_{RC}	Read cycle			350			250			450			ns
t_A	Access time					350			250			450	ns
t_{CO}		Output time	Chip enable			180			130			230	ns
	Previous read data valid with respect to												ns
t_{OH1}	Address			40			40			40			
t_{OH2}	Chip enable			0			0			0			
	WRITE CYCLE												
t_{WC}	Write cycle			350			250			450			ns
t_{WP}	Write pulse width			250			180			300			ns
t_{WR}	Write recovery time			20			20			20			ns
	Setup and hold time												ns
t_{AW}	Setup time	Write	Address	20			20			20			
t_{DW}	Setup time	Output	Data	250			180			300			
t_{DH}	Hold time	Output	Data	0			0			0			
t_{CW}	Setup time	Write	Chip enable	250			180			300			

NOTES on following page.

NOTES

1. Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only and functional operation of the device of these or any other condition above those indicated in the operation sections of this specification is not implied.
2. For operating at elevated temperatures the device must be derated based on a +150°C maximum junction temperature and a thermal resistance of 150°C/W junction to ambient (B package).
3. Typical values are at +25°C and typical supply voltages.
4. All inputs protected against static charge.
5. Parameter valid over operating temperature range unless otherwise specified.
6. All voltage measurements are referenced to ground.
7. Manufacturer reserves the right to make design and process changes and improvements.

TIMING DIAGRAMS