2518-N • 2519-N

DESCRIPTION

The 2518 32-bit and the 2519 40-bit recirculating static shift registers consist of enhancement mode p-channel silicon gate MOS devices intergrated on a single monolithic chip. Internal recirculation logic plus TTL/DTL level clock signals are provided for maximum interfacing ease.

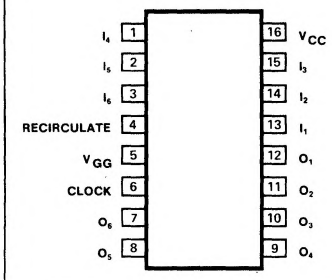
TRUTH TABLE

RECIR-CULATE	INPUT	FUNCTION
1	0	Recirculate
1	1	Recirculate
0	0	"0" is written
0	1	"1" is written

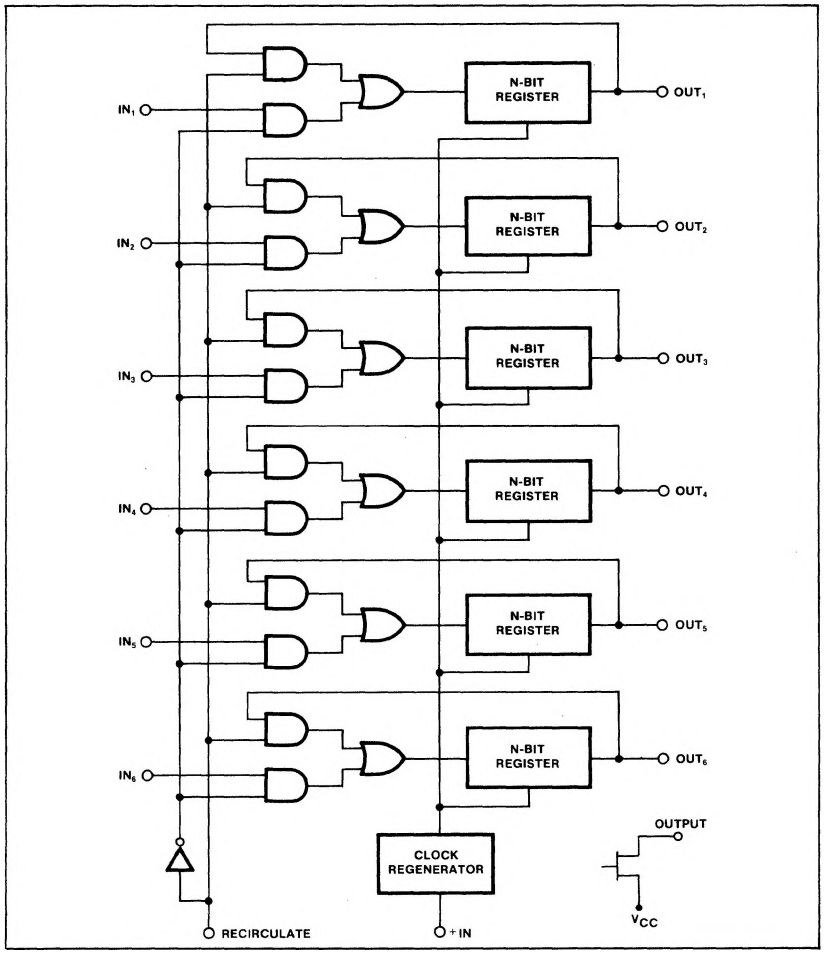
Data is read out when output enable is low. Output is tri-stated when output enable is high.

PIN CONFIGURATION

N PACKAGE



BLOCK DIAGRAM



ABSOLUTE MAXIMUM RATINGS[1]

	PARAMETER	RATING	UNIT
	Temperature range		°C
T_A	Operating[2]	0 to +70	
T_{STG}	Storage	-65 to 150	
P_D	Power dissipation at T_A = 70°C	640	mW
	Data and clock input voltages and supply voltages with respect to V_{CC}	0.3 to -20	V

DC ELECTRICAL CHARACTERISTICS

T_A = 0°C to +70°C, V_{CC} = +5V ± 5%, V_{GG} = -12V ± 5% unless otherwise specified.[3,4,5,6,7]

PARAMETER		TEST CONDITIONS	LIMITS			UNIT
			Min	Typ	Max	
	Input voltage[8]					V
V_{IL}	Low				0.6	
V_{IH}	High		3.4		5.3	
V_{ILC}	Clock low				0.6	
V_{IHC}	Clock high		3.4		5.3	
	Output voltage					V
V_{OL}	Low	I_{OL} = 1.6mA		0.5		
V_{OH}	High	I_{OH} = 100μA	3.8			
	Leakage current	T_A = 25°C				nA
I_{LO}	Output			10	1000	
I_{LC}	Clock	V_{ILC} = GND		10	500	
I_{LI}	Input load current	V_{IN} = -5.5V, T_A = 25°C		10	500	nA
I_{GG}	Supply current	Continuous operation, T_A = 25°C, f = 1.5MHz		16	25	mA
	Capacitance	At 1MHz, V_{AC} = 25mV p-p				pF
C_{IN}	Input	V_{IN} = V_{CC}		5	7	
C_ϕ	Clock	V_ϕ = V_{CC}		6	7	

AC ELECTRICAL CHARACTERISTICS

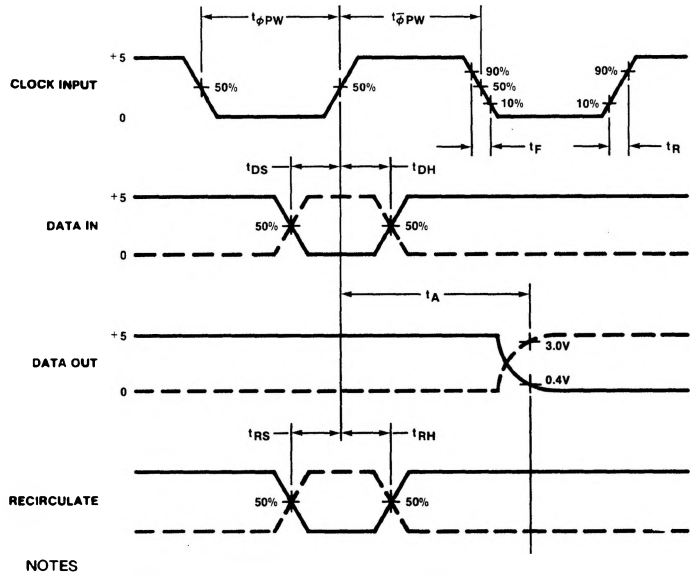
T_A = 0°C to +70°C, V_{CC} = +5V ± 5%, V_{GG} = -12V ± 5%, V_{ILC} = 0.4V to 4.0V

PARAMETER		TO	FROM	LIMITS			UNIT
				Min	Typ	Max	
Freq.	Clock rep rate			dc	3	2	MHz
	Pulse width						μs
$t_{\phi PW}$	Clock[10]			.300		100	
$\overline{t_{\phi PW}}$	$\overline{\text{Clock}}$			.200		dc	
	Setup and hold time						ns
t_{DS}	Setup time	Clock in	Data in	100			
t_{DH}	Hold time	Data in	Clock in	70			
t_{RS}	Setup time	Clock	Recirculate	150			
t_{RH}	Hold time	Recirculate	Clock	50			
t_R,t_F	Clock pulse transition					5	μs
t_A	Clock to data out delay	Data	Clock		300	350	ns

NOTES

1. Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or at any of this specification is not implied.
2. For operating at elevated temperatures the device must be derated based on a 150°C maximum junction temperature and a thermal resistance of 125°C C/W, junction to ambient.
3. All inputs are protected against static charge.
4. Parameters are valid over operating temperature range unless specified.
5. All voltage measurements are referenced to ground.
6. Manufacturer reserves the right to make design and process changes and improvements.
7. Typical values are at +25°C and typical supply voltages.
8. Guaranteed input levels are stated for worst case conditions including a ±5% variation in V_{CC} and a temperature variation of 0°C to +70°C. Actual input requirements with respect to V_{CC} are V_{IH} = V_{CC} -1.85V and V_{IL} = V_{CC} - 4.15V.
9. V_{OL} is dependent on R_L and input characteristics of driven gate.
10. Input rise and fall times = 10ns. Output load is 1 TTL gate.
11. For static operation, clock must be stopped in TTL high state in order to retain data (see clock pulse width specification).

TIMING DIAGRAM



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