signetics

512 AND 1024 BIT RECIRCULATING DYNAMIC SHIFT REGISTERS

2524
2525

SILICON GATE MOS 2500 SERIES

DESCRIPTION

These Signetics 2500 Series 512 and 1024 bit recirculating dynamic shift registers consist of enhancement mode P-channel MOS devices integrated on a single monolithic chip. Internal recirculation logic plus write and read controls are included on the chip.

FEATURES

- HIGH FREQUENCY OPERATION-5 MHz Typical Clock Rate
- SINGLE 512, SINGLE 1024
- TTL, DTL COMPATIBLE
- WRITE AND READ CONTROLS INCLUDED
- LOW POWER DISSIPATION-150μW/bit at 1 MHz
- LOW CLOCK CAPACITANCE-80pF for 512, 160pF for 1024 Bits
- +5, -5 POWER SUPPLIES
- STANDARD PACKAGE 8-LEAD DIP
- SIGNETICS P-MOS SILICON GATE PROCESS TECHNOLOGY

APPLICATIONS

FAST ACCESS SWAPPING MEMORY SYSTEMS
LOW COST SEQUENTIAL ACCESS MEMORIES
LOW COST BUFFER MEMORIES
CRT REFRESH MEMORIES
DELAY LINE MEMORY REPLACEMENT
DRUM MEMORY REPLACEMENT

PROCESS TECHNOLOGY

Use of low threshold *silicon gate technology* allows high speed (5MHz typical) while reducing power dissipation and clock input capacitance dramatically as compared to other technologies. The use of low voltage circuitry minimizes power dissipation and facilitates interfacing with bipolar integrated circuits.

BIPOLAR COMPATIBILITY

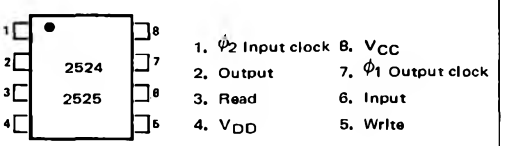
The signal inputs of these registers can be driven directly by standard bipolar integrated (TTL, DTL, etc.) or by MOS circuits. The bare drain output stage provides driving capability for both MOS and bipolar integrated circuits (one standard TTL load).

SILICONE PACKAGING

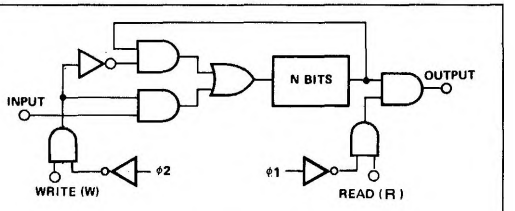
Low cost silicone DIP packaging is implemented and reliability is assured by the use of Signetics unique silicon gate MOS process technology. Unlike the standard metal gate MOS process the silicon material over the gate oxide passivates the MOS transistors, and the deposited dielectric material over the silicon gate-oxide-substrate structure provides an ion barrier. In addition, Signetics proprietary surface passivation and silicone packaging techniques result in an MOS circuit with inherent high reliability and demonstrating superior moisture resistance, mechanical shock and ionic contamination barriers.

PIN CONFIGURATION (Top View)

V PACKAGE



BLOCK DIAGRAM



NOTE
N = 512 or 1024 '0' = 0V, '1' = +5V.

TRUTH TABLE

WRITE	READ	FUNCTION
0	0	Recirculate, Output is '0'
0	1	Recirculate, Output is Data
1	0	Write Mode, Output is '0'
1	1	Read Mode Output is Data

PART IDENTIFICATION TABLE

PART NO.	BIT LENGTH	PACKAGE
2524V	512	8 pin DIP
2525V	1024	8 pin DIP

MAXIMUM GUARANTEED RATINGS (1)

Operating Ambient Temperature (2)	0°C to +70°C
Storage Temperature	−65°C to +150°C
Power Dissipation (2)	535mW@T_A>70°C
Data and Clock Input Voltages and Supply Voltages with respect to V_{CC}	+ 0.3V to −20V

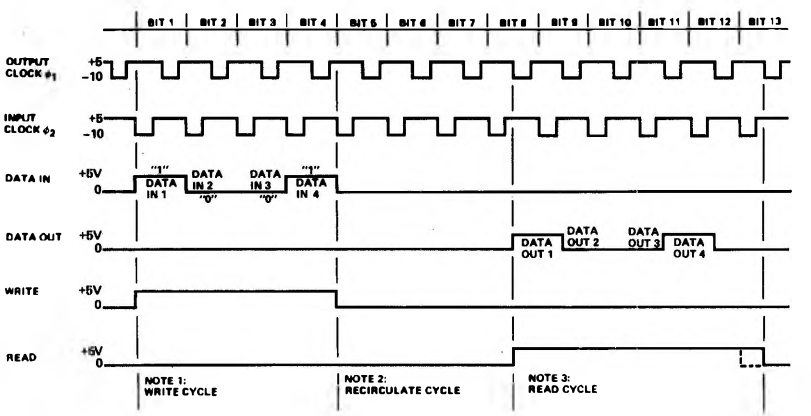
NOTES:

1. Stresses above those listed under "Maximum Guaranteed Rating" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or at any other condition above those indicated in the operational sections of this specification is not implied.
2. For operating at elevated temperatures the device must be derated based on a +150°C maximum junction temperature and a thermal resistance of 150°C/W junction to ambient.
3. All inputs are protected against static charge.
4. See "Minimum Operating Frequency" graph for low limits on data rep. rate.
5. All voltage measurements are referenced to ground.
6. Manufacturer reserving the right to make design and process changes and improvements.
7. Typical values are at +25°C and nominal supply voltages.
8. Parameters are valid over operating temperature range unless otherwise specified.
9. V_{CC} tolerance is ± 5%. Any variation is actual V_{CC} will be tracked directly by V_{IL}, V_{IH} and V_{OH} which are stated for a V_{CC} of exactly 5 volts.
10. V_{OL} is a function of the input characteristics of the driven TTL/DTL gate I_{OI} and V_{CLAMP} and the value of the pull-down resistor (R_L).

DC CHARACTERISTICS T_A = 0°C to +70°C; V_{CC} = +5V(9); V_{DD} = 5V ±5% unless otherwise noted.

SYMBOL	TEST	MIN	TYPICAL	MAX	UNIT	CONDITION
I_{LI}	Input Load Current		10	500	nA	V_{IN} =-5.5V; T_A = 25°C
I_{LO}	Output Leakage Current		10	1000	nA	$V_{\phi 1}$ = $V_{\phi 2}$ = -12V; V_{DD} = -5 V_{OUT} =-5.5V; T_A = 25°C
I_{LC}	Clock Leakage Current		10	1000	nA	V_{ILC} = -12V ; T_A = 25°C
I_{DD}	Power Supply Current: 2524		15	35	mA	Continuous Operation; ϕpW = 150nS; 1MHz
	2525		25	35	mA	V_{ILC} = -12V; T_A = 25°C V_{DD} = -5.5V
V_{IL}	Input "Low" Voltage	-5.0		1.05	V	
V_{IH}	Input "High" Voltage	3.2		5.3	V	
V_{ILC}	Clock Input "Low" Voltage	-12.0		-10.0	V	
V_{IHC}	Clock Input "High" Voltage	4.0		5.3	V	

TIMING DIAGRAM



NOTE:
This is a simplified illustration of the timing of a 4 bit recirculating shift register showing the 3 basic modes of operation.

NOTE 1: (WRITE cycle)

The positive and negative going edge of the "Write" control is coincident with the negative going edge of the input clock (ϕ_2). The "Read" control may be either "1" or "0"

NOTE 2: (RECIRCULATE cycle)

Data recirculates if the "Write" control line is "0". "Read" may be either "1" or "0".

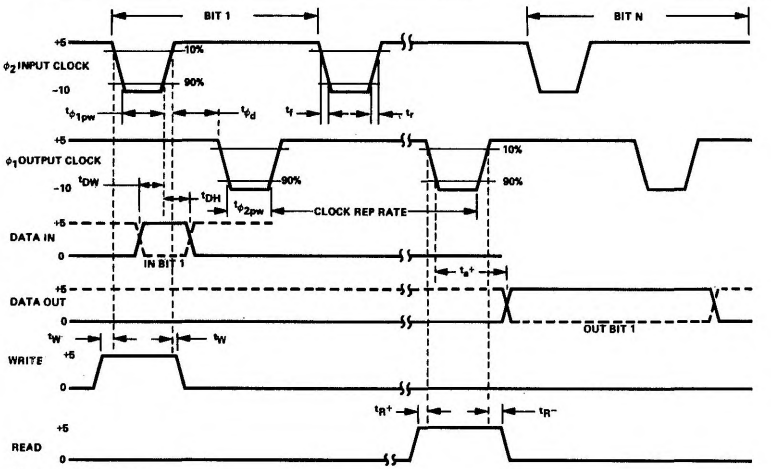
NOTE 3: (READ cycle)

The positive going edge of the "Read" control is coincident with the negative edge of the output clock (ϕ_1). The negative going edge of "Read" is coincident with the negative going edge of either clock pulse succeeding the last desired data output bit. "Write" may be either "1" or "0"

CONDITIONS OF TEST

Input rise and fall times: 10 sec Output load is 1 TTL gate

TIMING DIAGRAM



NOTE:

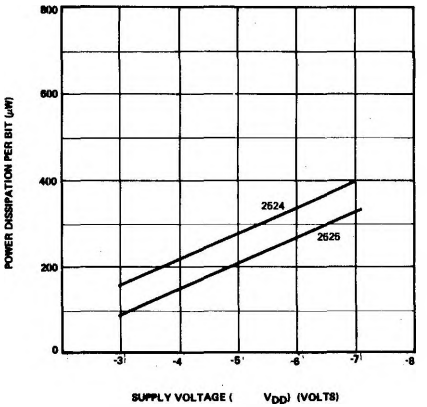
1. N = 512 for 2524 N= 1024 for 2525
2. Note that the Read Input is AND'ed with $\overline{\phi}_1$; therefore this function is not valid until ϕ_1 occurs.

AC CHARACTERISTICS $T_A = +25°C$ $V_{CC} = +5V(9)$; $V_{DD} = -5V \pm 5\%$; $V_{ILC} = -11V$

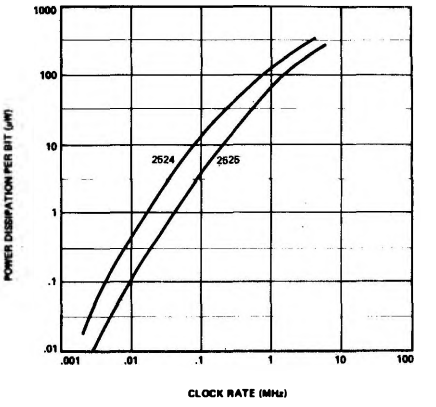
SYMBOL	TEST	MIN	TYP	MAX	UNIT	CONDITIONS
Frequency	Clock Data Rep Rate	.0005 (Note 4)	5	3	MHz	W = R = V_{CC}
$t_{\phi pw}$	Clock Pulse Width	135	85		ns	
$t_{\phi d}$	Clock Pulse Delay	10			ns	
t_r;t_f	Clock Pulse Transition	10		1000	ns	
t_{DW}	Data Write (Setup) Time	70			ns	
t_{DH}	Data to Clock Hold Time	20			ns	
t_{a+}	Clock to Data Out Delay			100	ns	
t_{R-}; t_{W-}	Clock to "Read" or "Write" Timing	0			ns	
t_{R-}; t_{W+}	Clock to "Read" or "Write" Timing	0			ns	
C_{in}	Input Capacitance			5	pF	1MHz; V_I=V_{CC};V_{AC}=25m V_{P-P}
C_{out}	Output Capacitance			5	pF	1MHz; V_0=V_{CC};V_{AC}=25m V_{P-P}
C_ϕ	Clock Capacitance 2524 2525			 80 160	 pF pF	1MHz; V=V_{CC}; V_{AC}=25m V_{P-P}
V_{OL}	Output "Low" Voltage		-1.0		V	R_L =3.0K; 1 TTL Load (I_L = 1.6mA) Note 10
V_{OH1}	Output "High" Voltage Driving 1 TTL Load	2.4	3.5		V	R_L=3.0K; 1 TTL Load (I_L=100μA)
V_{OH2}	Output "High" Voltage Driving MOS	3.6	4.0		V	R_L = 5.6K; C_L = 10pF

CHARACTERISTIC CURVES

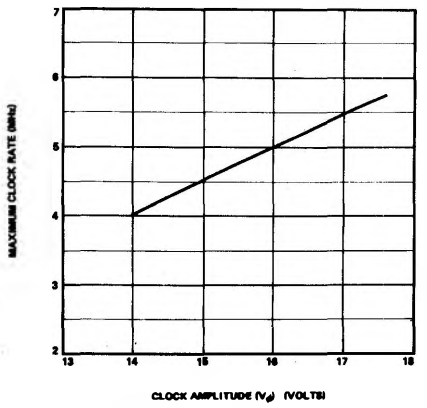
POWER DISSIPATION/BIT VERSUS SUPPLY VOLTAGE



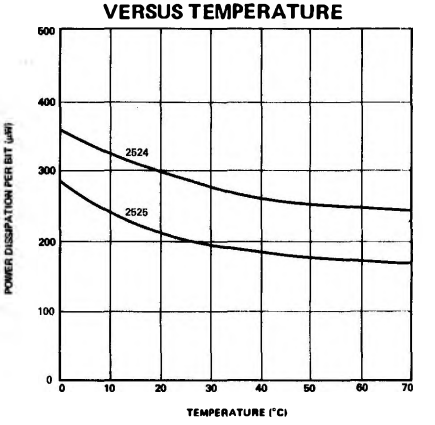
POWER DISSIPATION/BIT VERSUS CLOCK RATE



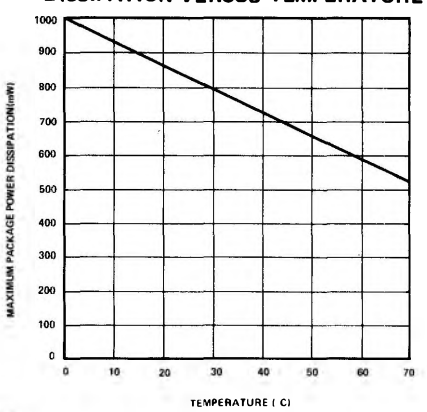
MAXIMUM CLOCK RATE VERSUS CLOCK AMPLITUDE



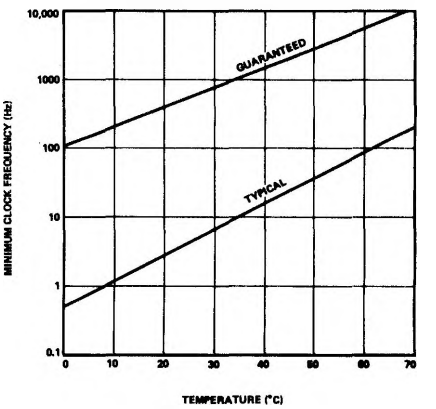
POWER DISSIPATION/BIT VERSUS TEMPERATURE



MAXIMUM PACKAGE POWER DISSIPATION VERSUS TEMPERATURE



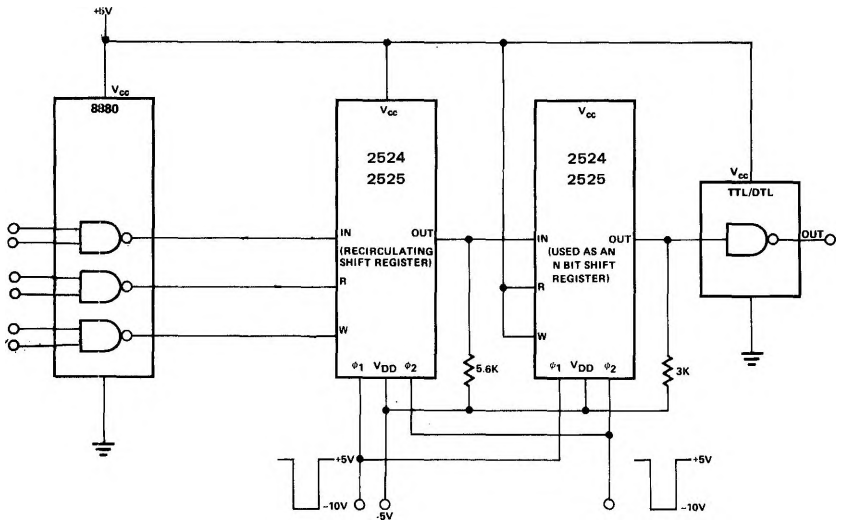
MINIMUM OPERATING CLOCK FREQUENCY VERSUS TEMPERATURE



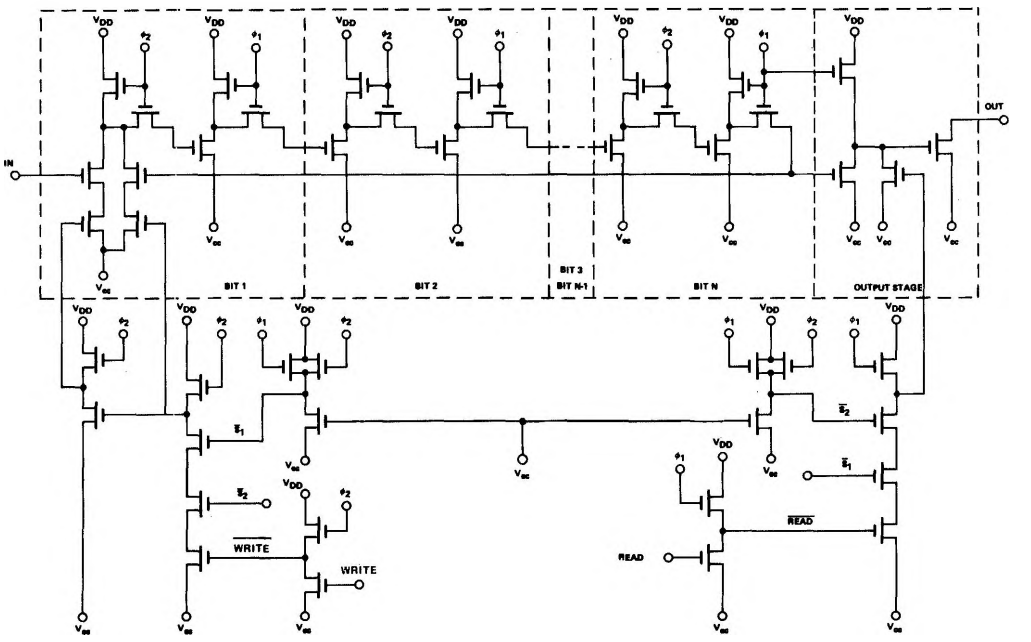
NOTE:
Conditions for typical curves: V_{CC} = +5V, V_{DD} = -5V, clock duty cycle = 35%, f_{CLK} = 3MHz, $V\phi_{p\text{-}p}$ = 16V, $\phi_{PW1} = \phi_{PW2}$ = 80ns, T_A = +25°C unless otherwise noted.

APPLICATIONS DATA

TTL/DTL/MOS INTERFACES



CIRCUIT SCHEMATIC



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