2532-N

DESCRIPTION

The 2532 static shift register consists of enhancement mode p-channel silicon gate MOS devices integrated on a single monolithic chip. Each of the four 80-bit registers is provided with an independent input, push-pull output and recirculation control. The single phase clock is common to all 4 registers. All inputs and outputs including the clock interface directly with TTL or DTL circuits without external components.

Data is entered when the clock is at a logic high. Data is shifted when the clock goes low. When the recirculate control is at a logic high, data recirculates and is continuously available at the output, data input is inhibited. When the recirculate control is at a logic low, data is entered.

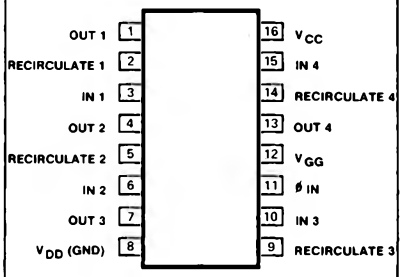
TRUTH TABLE

RECIRCULATE	FUNCTION	INPUT
0	"0" is written	0
0	"1" is written	1
1	Recirculate	0
1	Recirculate	1

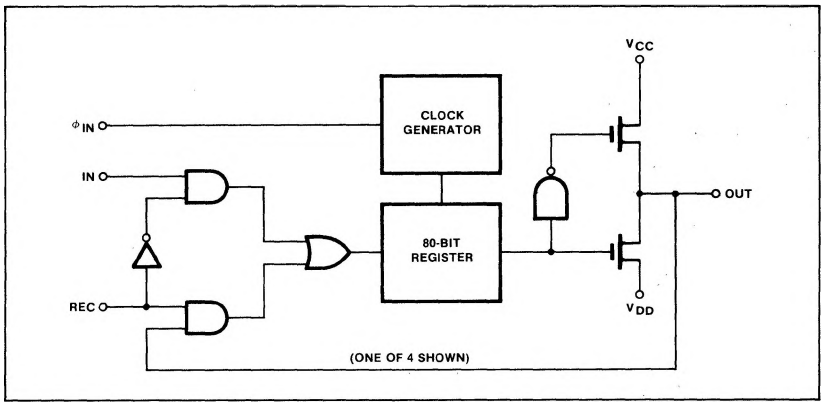
"0" = OV, "1" = +5V

PIN CONFIGURATION

N PACKAGE



BLOCK DIAGRAM



ABSOLUTE MAXIMUM RATINGS[1]

PARAMETER		RATING	UNIT
	Temperature range		°C
T_A	Operating[2]	0 to 70	
T_{STG}	Storage	-65 to 150	
P_D	Power dissipation at $T_A = 70°C$	640	mW
	Data and clock input voltages and supply voltages with respect to V_{CC}	+0.3 to -20	V

DC ELECTRICAL CHARACTERISTICS

T_A = 0°C to 70°C, V_{CC} = 5V ± 5%, V_{GG} = -12V ± 5% unless otherwise specified.

PARAMETER		TEST CONDITIONS	LIMITS			UNIT
			Min	Typ	Max	
	Input voltage[3]					V
V_{IL}	Low				0.6	
V_{IH}	High		3.4		5.3	
V_{ILC}	Clock low				0.6	
V_{IHC}	Clock high		3.4		5.3	
	Output voltage					V
V_{OL}	Low	I_{OL} = 1.6mA			0.5	
V_{OH}	High	I_{OH} = 100μA	3.8			
	Supply current					mA
I_{GG}		Continous operation, f = 1.5MHz, T_A = 25°C, Outputs open		6	10	
I_{CC}				12	20	
I_{LI}	Input load current	V_{IN} - 5.5V, T_A -25°C		10	500	nA
I_{LC}	Clock leakage current	V_{ILC} = OV, T_A = 25°C		10	500	nA
	Capacitance	At 1MHz, V_{AC} = 25mV p-p				pF
C_{IN}	Input	V_{IN} = V_{CC}			5	
C_ϕ	Clock	V_ϕ = V_{CC}			5	

AC ELECTRICAL CHARACTERISTICS

T_A = 0°C to 70°C, V_{CC} = 5V ± 5%, V_{GG} = -12V ± 5%,
Input rise and fall times = 10ns, Output load = 1TTL gate

PARAMETER		TO	FROM	TEST CONDITIONS	LIMITS			UNIT
					Min	Typ	Max	
Freq.	Clock rep rate			See timing diagram	dc	3.0	1.5	MHz
	Pulse width							μs
$t_{\phi PW}$	Clock				0.33		100	
$t_{\bar{\phi}PW}$	$\overline{\text{Clock}}$				0.33		dc	
t_R,t_F	Clock pulse transition						5	μs
	Setup and hold time							ns
t_{DS}	Setup time	ϕin	Data in		120			
t_{DH}	Hold time	Data in	ϕin		70			
t_{RS}	Setup time	ϕin	Recirculate		150			
t_{RH}	Hold time	Recirculate	ϕin		70			
t_A	Delay time	Data out	Clock	I_{OL} = 1.6mA			400	ns

NOTES

1. Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or at any other condition above those indicated in the operational sections of this specification is not implied.
2. For operating at elevated temperatures the device must be derated based on a 150°C maximum junction temperature and a thermal resistance of 125°C/W junction to ambient.
3. Guaranteed input levels are stated for worst case conditions including a ±5% variation in V_{CC} and a temperature variation of 0°C to +70°C. Actual input requirements with respect to V_{CC} are V_{IH} = V_{CC} -1.85V and V_{IL} = V_{CC} -4.15V.
4. All inputs are protected against static charge.
5. Parameters are valid over operating temperature range unless specified.
6. All voltage measurements are referenced to ground.
7. Manufacturer reserves the right to make design and process changes and improvements.
8. Typical values are at +25°C and typical supply voltages.

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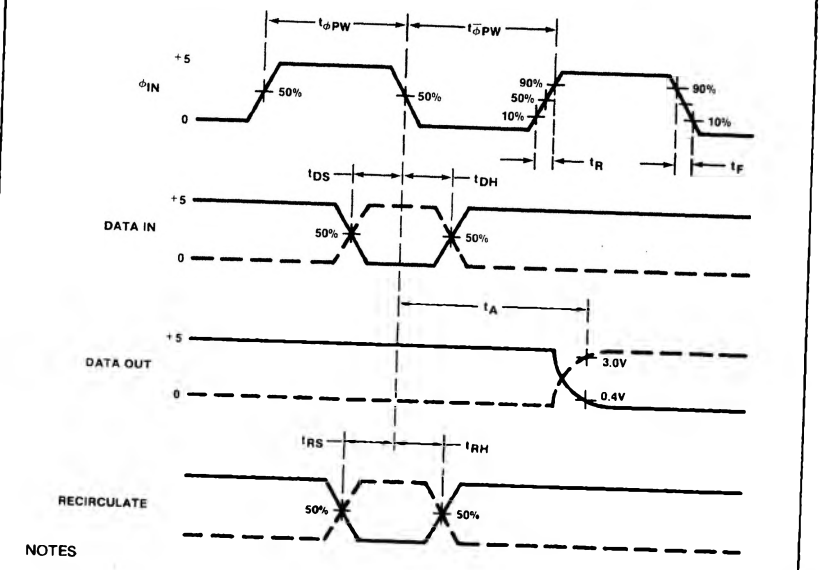
TIMING DIAGRAM



NOTES

A. $t_R = t_F$ 10ns for all inputs.
B. Clock must be stopped in the TTL low state to retain data during static operation.