2533-N

DESCRIPTION

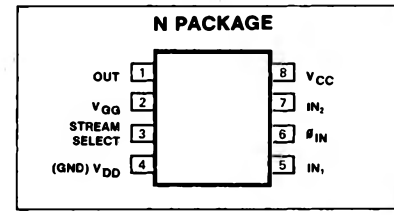
The 2533 static shift register consists of enhancement mode p-channel silicon gate MOS devices integrated on a single monolithic chip.

The 1024-bit register is equipped with 2 data inputs together with a stream select control to facilitate external recirculation.

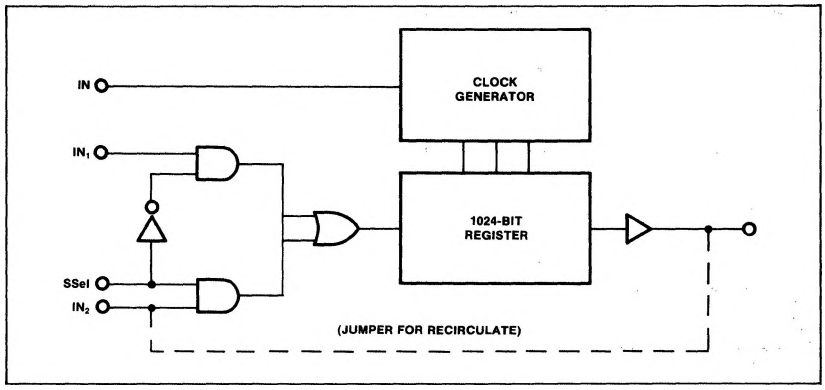
The single phase clock input, data input, data output, and stream select control will interface directly with TTL/DTL circuits without external components.

Data is entered when the clock is at a logic high. Data is shifted when the clock goes low.

PIN CONFIGURATION



BLOCK DIAGRAM



TRUTH TABLE

STREAM SELECT	FUNCTION
0	IN 1 selected
1	IN 2 selected

"0" = 0V, "1" = +5V

ABSOLUTE MAXIMUM RATINGS[1]

	PARAMETER	RATING	UNIT
	Temperature range[2]		°C
T_A	Operating	0 to 70	
T_{STG}	Storage	-65 to 150	
P_D	Power dissipation at $T_A > 25°C$[2]	535	mW
	Data and clock input voltages and supply voltages with respect to V_{CC}	0.3 to -20	V

DC ELECTRICAL CHARACTERISTICS

$T_A = 0°C$ to 70°, $V_{CC} = 5V \pm 5\%$, $V_{GG} = -12V + 5\%$ unless otherwise specified.

	PARAMETER	TEST CONDITIONS	LIMITS Min	LIMITS Typ	LIMITS Max	UNIT
	Input voltage[3]	$V_{CC} = 5V$				V
V_{IL}	Low				0.6	
V_{IH}	High		3.4		5.3	
V_{ILC}	Clock low				0.6	
V_{IHC}	Clock high		3.4		5.3	
	Output voltage					V
V_{OL}	Low	$I_{OL} = 1.6mA$			0.5	
V_{OH}	High	$I_{OH} = 100\mu A$	3.8			
I_{LI}	Input load current	$V_{IN} = 0$, $T_A = 25°C$		10	500	nA
I_{LC}	Clock leakage current	$V_{ILC} = GND$, $T_A = 25°C$		10	500	nA
	Supply current	Continuous operation, f = 1.5MHz				mA
I_{CC}				16	30	
I_{GG}				5.0	7.5	
	Capacitance	At 1MHz; $V_{AC} = 25mV$ p-p				pF
C_{IN}	Input	$V_{IN} = V_{CC}$			5	
C_{OUT}	Output	$V_{OUT} = V_{CC}$			5	
C_ϕ	Clock	$V_\phi = V_{CC}$			5	

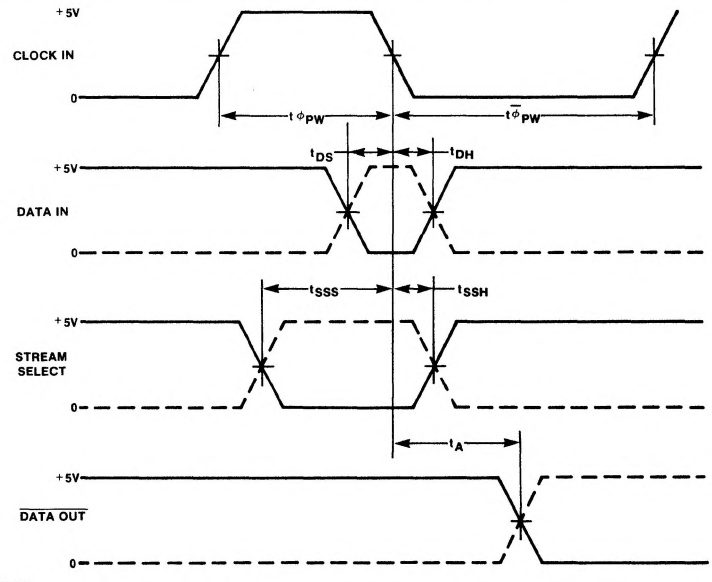
AC ELECTRICAL CHARACTERISTICS $T_A = 25°C$, $V_{CC} = 5V \pm 5\%$, $V_{GG} = -12V \pm 5\%$

PARAMETER		TO	FROM	TEST CONDITIONS	LIMITS			UNIT
					Min	Typ	Max	
	Clock and data rep rate			See timing diagram		2	1.5	MHz
	Pulse width							
$t_\phi PW$	Clock				.350		100	μs
$t_{\overline{\phi}} PW$	Clock				250		dc	ns
t_R, t_F	Clock pulse transition						1	μs
	Setup and hold time							ns
t_{DW}	Setup time	Write	Data		50			
t_{DH}	Hold time	Clock	Data		70			
t_{SSS}	Setup time	Clock in	Stream select		80			
t_{SSH}	Hold time	Stream select	Clock in		50			
t_A	Delay time	Data out	Clock			200	300	ns

NOTES

1. Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or at any other condition above those indicated in the operational sections of this specification is not implied.
2. For operating at elevated temperatures the device must be derated corresponding to a thermal resistance of 150°C/W junction to ambient.
3. Guaranteed input levels are stated for worst case conditions including a ±5% variation in V_{CC} and a temperature variation of 0°C to +70°C. Actual input requirements with respect to V_{CC} are $V_{IH} = V_{CC} - 1.85V$ and $V_{IL} = V_{CC} - 4.15V$.
4. All inputs are protected against static charge.
5. Parameters are valid over operating temperature range unless specified.
6. All voltage measurements are referenced to ground.
7. Manufacturer reserves the right to make design and process changes and improvements.
8. Typical values are at +25°C and typical supply voltages.

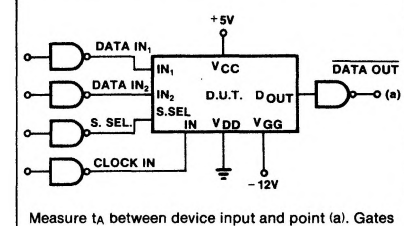
TIMING DIAGRAM



NOTES

A. Times measured at 50% points with input t_R $t_F \leq 10ns$.
B. Clock must be stopped in TTL low state to retain data during static mode operation.

TEST LOAD CIRCUIT



Measure t_A between device input and point (a). Gates are standard 7400.