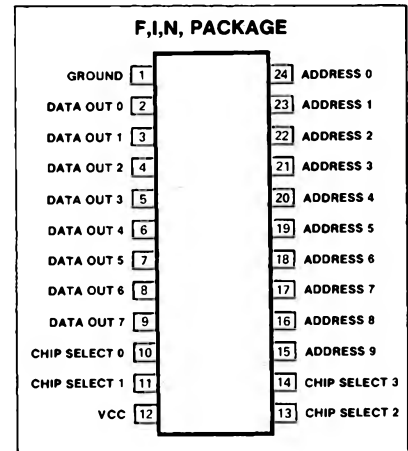


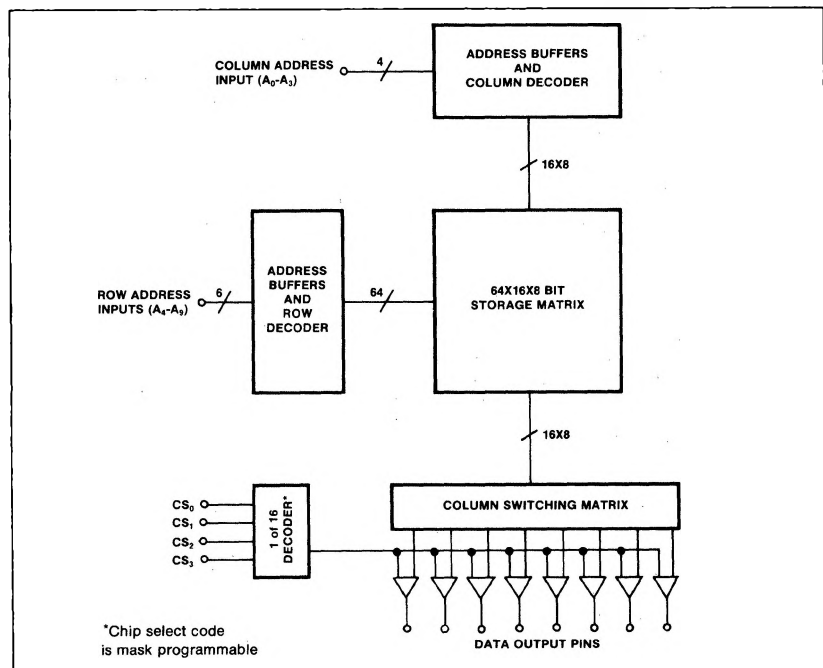
FEATURES

- Static operation—no clocks
- Access time:
2608: 550ns
2608-1: 450ns
- Single 5V power supply and ground power connections
- TTL compatible inputs and outputs
- Power dissipation: 400mW max
- Tri-state outputs
- 4 mask programmable chip selects for easy word expansion
- Low threshold n-channel silicon gate technology which allows ease of use with low voltage logic families such as transistor-transistor logic
- Standard 24-pin package
- Fully decoded

PIN CONFIGURATION



BLOCK DIAGRAM



ABSOLUTE MAXIMUM RATINGS^{1,2}

	PARAMETER	RATING	UNIT
T _A	Temperature range		°C
	Operating	0 to 70	
T _{STG}	Storage	-65 to 150	
	All input, output and supply voltages with respect to ground pin	-0.5 to 7	V

DC ELECTRICAL CHARACTERISTICS $T_A = 0^\circ\text{C}$ to $+70^\circ\text{C}$, $V_{CC} = +5V \pm 5\%$ (unless otherwise noted)^{3,4,5,6,7}

PARAMETER	TEST CONDITIONS	LIMITS			UNIT
		Min	Typ	Max	
V_{IL} V_{IH}	Input voltage Low High	-0.5 2.2		0.65	V
V_{OL} V_{OH}	Output voltage Low High			0.45	V
I_{IN}	Input load current			10	μA
I_{LOH} I_{LOL}	Output leakage current	Device deselected $V_O = 2.4V$ $V_O = 0.4V$		10 10	μA
I_{CC}	Supply current	$V_{CC} = 5.25V$, $T_A = 0^\circ\text{C}$		80	mA
C_{IN} C_{OUT}	Capacitance Input Output	$V_{IN} = 0V$ $V_{OUT} = 0V$		7.5 15	pF

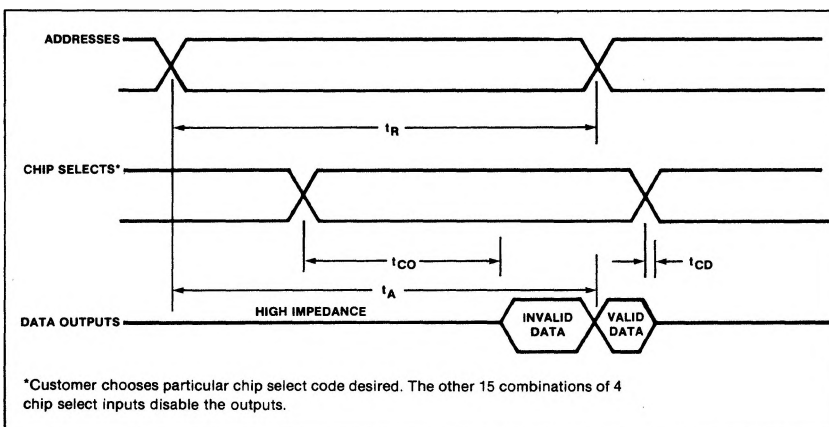
AC ELECTRICAL CHARACTERISTICS $T_A = 0^\circ\text{C}$ to $+70^\circ\text{C}$, $V_{CC} = +5V \pm 5\%$ ^{8,9,10}

PARAMETER	TO	FROM	2608			2608-1			UNIT
			Min	Typ	Max	Min	Typ	Max	
t_R	Read cycle time		550			450			ns
t_{CO}	Enable time ¹¹	Output			300			300	ns
t_{CD}	Disable time ¹¹	Output	10		150	10		150	ns
t_A	Access time ¹¹	Output	100		550	100		450	ns

NOTES

- Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or at any other condition above those indicated in the operation sections of this specification is not implied.
- For operating at elevated temperatures the device must be derated based on a $+150^\circ\text{C}$ maximum junction temperature and a thermal resistance of 50°C/W junction to ambient.
- This product includes circuitry specifically designed for the protection of its internal devices from the damaging effects of excessive static charge. Nonetheless, it is suggested that conventional precautions be taken to avoid applying any voltages larger than the rated maxima.
- Parameter valid over operating temperature range unless otherwise specified.
- All voltage measurements are referenced to ground.
- Manufacturer reserves the right to make design and process improvements.
- Typical values are at $+25^\circ\text{C}$, typical supply voltages, and typical processing parameters.
- Input levels swing between 0.65V and 2.2V.
- Input signal transition times are 20ns.
- Timing reference level is 1.5V.
- Output load is one standard TTL load plus 130pF.

TIMING DIAGRAM



PIN DESCRIPTION

Addresses

These 10 TTL-compatible inputs are decoded on-chip to select one of 1024 8-bit bytes. Since the 2608 utilizes static logic throughout, a change in addresses results in a change in data as long as the chip is selected. Access time is measured from the point where the last address input became stable. Cycle time and access time are equal in a static ROM design.

Chip Selects

There are 4 TTL-compatible chip select inputs for the 2608. Only 1 combination of these 4 signals enables the chip. The other 15 disable the chip. The particular enabling combination is chosen by the customer and specified on the first punched card of the customer card deck. A positive logic convention is assumed.

Data Outputs

The 8 data outputs are push-pull buffers capable of driving one standard TTL load plus a 130pF load capacitance. These outputs are placed in the high impedance state when any one of the disabling combinations of the chip select inputs is present.

CODING FORMAT

Coding data for the 2608 may be sent to Signetics via punched cards or via a written truth table. Cards are preferred since errors are essentially eliminated.

On receipt of a card deck, Signetics will translate the card deck to a truth table using the Signetics Computer Aided Design (CAD) facility. The truth table will then be sent to the customer for final approval. On receipt of final approval, Signetics will produce masks and proceed with manufacturing.

DATA CARDS

- Columns 12-75 Hexadecimal data coding
- 77-78 Card number (starting 01)
- 79-80 Total number of cards (32)

Column 12 on the first card contains the hexadecimal equivalent of bits D7 thru D4 of byte 0, while column 13 contains the hexadecimal equivalent of bits D3 thru D0. Columns 14 and 15 contain byte 1, columns 16 and 17 byte 2, and so on.

The first card contains the first 32 bytes. Columns 12 and 13 on the second card will contain byte 32 (the 33rd byte). A total of 32 cards will contain 1024 bytes of 8 bit.

CARD FORMAT

IDENTIFICATION CARDS
 Column 8, 9 Custom designation "CN"
 Column 10, 11, 12, 13, Custom number (assigned by Signetics)
 Column 15, 16, 17, 18, 19 "Coded"
 Column 21, 22, 23, 24 Chip select code (CS3, 2, 0)
 Column 26-80 Customer identification

Person responsible for reviewing Signetics computer generated truth table

Street address

City State Zip

Company name

BINARY TO HEXADECIMAL CONVERSION

BINARY COMBINATION D0-D3 or D7-D4				HEXA- DECIMAL CHARACTER
0	0	0	0	0
0	0	0	1	1
0	0	1	0	2
0	0	1	1	3
0	1	0	0	4
0	1	0	1	5
0	1	1	0	6
0	1	1	1	7
1	0	0	0	8
1	0	0	1	9
1	0	1	0	A
1	0	1	1	B
1	1	0	0	C
1	1	0	1	D
1	1	1	0	E
1	1	1	1	F