## DESCRIPTION

The Signetics 2616 is a 16,384-bit static MOS read-only memory organized as 2048 words by 8 bits. This ROM is designed for memory applications where high performance, large bit storage, and simple interfacing are important design objectives.

The inputs and outputs are fully TTL compatible. This device operates with a single 5V power supply. The three chip select inputs are programmable. Any combination of active high or low level chip select inputs can be defined by the designer and the desired chip select logic level is fixed during the masking process. These three programmable chip select inputs, as well as OR-tie compatibility on the outputs, facilitates easy memory expansion.

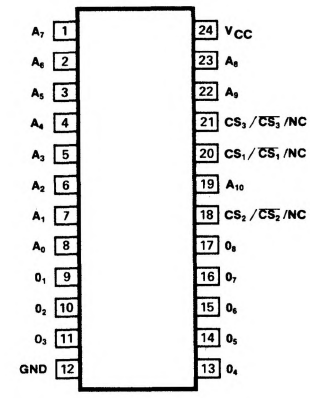
The 2616 read-only memory is fabricated with n-channel silicon gate technology. This technology provides the designer with high performance, easy-to-use MOS circuits. Only a single 5V power supply is needed and all devices are directly TTL compatible.

## FEATURES

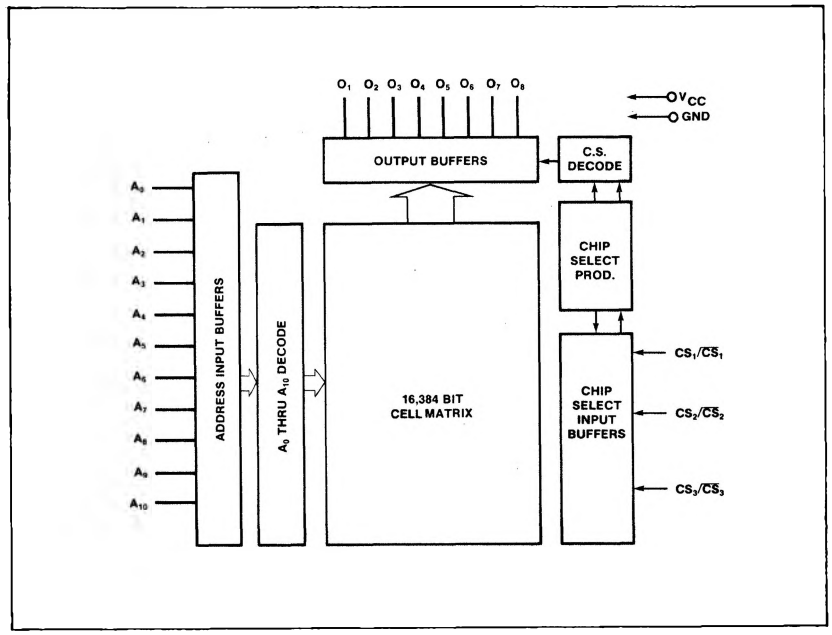
- **Single 5V power supply**
- **Guaranteed 350/450ns access time**
- **Directly TTL compatible—all inputs and outputs**
- **Three programmable chip select inputs for easy memory expansion or no connection option**
- **Three-state output—OR-tie capability**
- **Fully decoded—on chip address decode**
- **Inputs protected—all inputs have protection against static charge**

## PIN CONFIGURATION

F,I,N PACKAGE




## BLOCK DIAGRAM




## ABSOLUTE MAXIMUM RATINGS[1]

| | PARAMETER | RATING | UNIT |
|---|---|---|---|
| | Temperature range | | °C |
| $T_A$ | Operating | 0 to 70 | |
| $T_{STG}$ | Storage | -65 to 150 | |
| | Supply voltage to ground potential | -0.5 to 7 | V |
| | Applied voltage | | V |
| | Input | -0.5 to 7 | |
| | Output | -0.5 to 7 | |
| $P_D$ | Power dissipation | 1 | W |

## DC ELECTRICAL CHARACTERISTICS

$T_A$ = 0°C to 70°C, $V_{CC}$ = 5.0V ± 5% unless otherwise specified

| PARAMETER | | TEST CONDITIONS | LIMITS | | | UNIT |
|---|---|---|---|---|---|---|
| | | | Min | Typ | Max | |
| | Input voltage[2] | | | | | V |
| $V_{IL}$ | Low | | -0.5 | | 0.8 | |
| $V_{IH}$ | High | | 2.2 | | $V_{CC}$ | |
| | Output voltage | $V_{CC}$ = 4.75V | | | | V |
| $V_{OL}$ | Low | $I_{OL}$ = 1.6mA | | | 0.4 | |
| $V_{OH}$ | High | $I_{OH}$ = -100μA | 2.4 | | $V_{CC}$ | |
| $I_{LI}$ | Input load current | $V_{CC}$ = 5.25V, OV ≤ $V_{IN}$ ≤ 5.25V | | | 10 | μA |
| $I_{LO}$ | Output leakage current | Chip deselected, $V_{OUT}$ = 0.4V to $V_{CC}$ | | | 10 | μA |
| $I_{CC}$ | Supply current | Output unloaded, $T_A$ = 25°C, $V_{CC}$ = 5.25V, $V_{IN}$ = $V_{CC}$ | | | 115 | mA |
| | Capacitance[3] | $T_A$ = 25°C, f = 1.0MHz, all pins except pin under test tied to ac ground | | | | pF |
| $C_{IN}$ | Input | | | | 7 | |
| $C_O$ | Output | | | | 10 | |

## AC ELECTRICAL CHARACTERISTICS

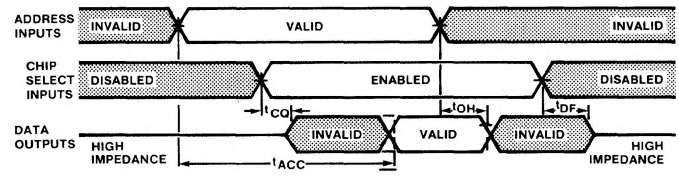
$T_A$ = 0°C to 70°C, $V_{CC}$ = 5.0V ± 5%, Output load = 1 TTL load and 100pF, Input transition time = 20ns, Timing reference levels: Input = 0.8V and 2.2V, Output = 0.4V and 2.4V unless otherwise specified.

| PARAMETER | | 2616 | | | 2616-1 | | | UNIT |
|---|---|---|---|---|---|---|---|---|
| | | Min | Typ | Max | Min | Typ | Max | |
| $t_{ACC}$ | Address access time | | | 450 | | | 350 | ns |
| $t_{CO}$ | Chip select delay | | | 200 | | | 150 | ns |
| $t_{DF}$ | Chip deselect delay | | | 200 | | | 150 | ns |
| $t_{OH}$ | Previous data valid after address change delay | 20 | | | 20 | | | ns |

NOTES

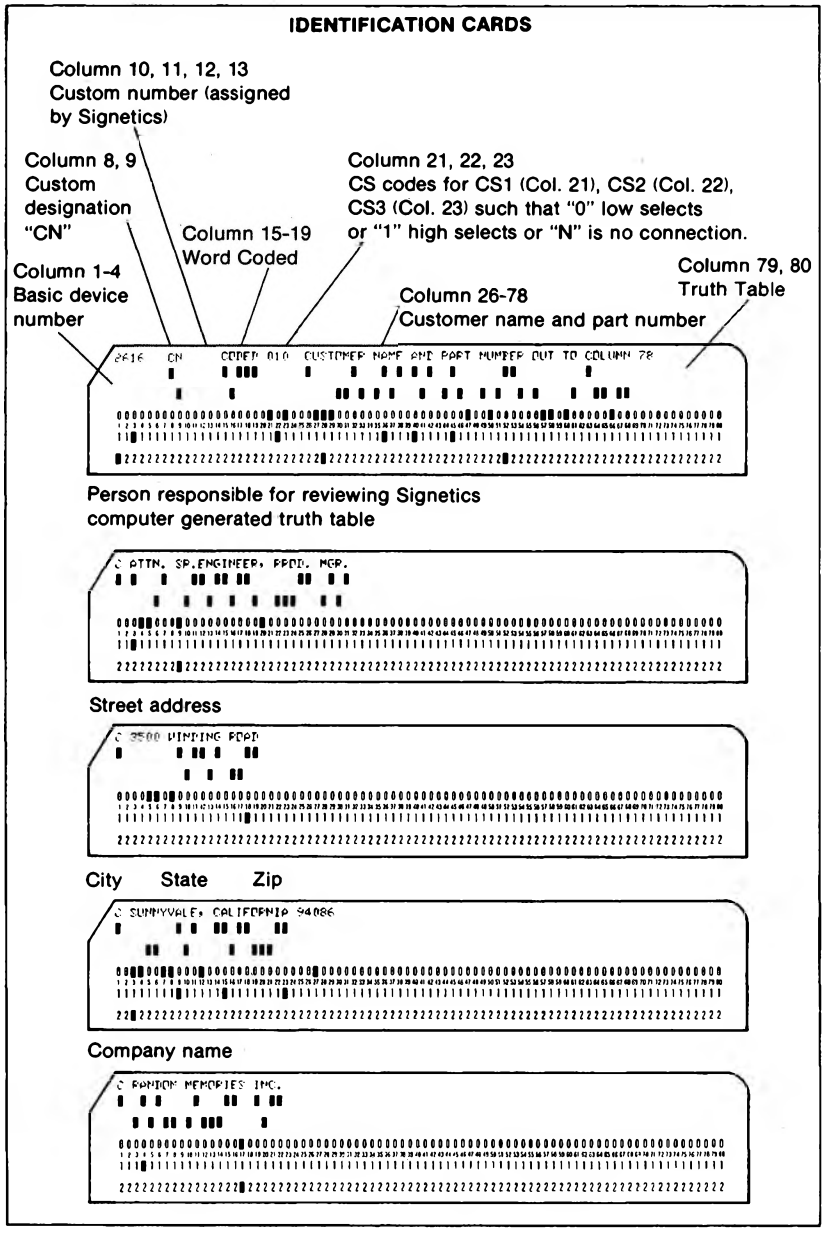
1. Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or at any other condition above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.
2. Input levels that swing more negative than -0.5V will be clamped and may cause damage to the device.
3. This parameter is periodically sampled and is not 100% tested.

## TIMING DIAGRAM



## CARD FORMAT

**IDENTIFICATION CARDS**




## PROGRAMMING INSTRUCTIONS

### 2616

All Signetics Read Only Memories utilize computer aided techniques to manufacture and test custom bit patterns. The custom bit pattern is supplied on standard 80 column computer cards in the format described below.

All address and related output patterns must be completely defined. Each deck of cards defining a specific ROM bit pattern consists of:

A. Title card
B. Comment cards
C. Data cards

For the user's convenience the data cards consisting of address and bit patterns can be specified in any one of three formats:

1. The hexadecimal format, where each data card carries (in hexadecimal) the initial input address for the 32 output words contained on that card, the 32 output words themselves (in hexadecimal) and the ROM truth table number. An N word ROM, therefore, requires n/32 cards, with all 32 output words defined on each card.
2. The octal format, where each data card carries (in octal) the initial input address for the 16 output words contained on that card, the 16 output words themselves (in octal) and the ROM truth table number. An N word ROM, therefore, requires N/16 cards, with all 16 output words defined on each card.
3. The binary format, where each data card carries (in decimal) the initial input address for the 8 output words contained on that card, the 8 output words themselves (in binary) and the ROM truth table number. An N word ROM, therefore, requires N/8 cards, with all 8 output words defined on each card.

Positive logic is used on all input cards; a logic "1" is the most positive voltage level and a logic "0" is the most negative level.

### Title Card

| COLUMN | INFORMATION |
|---|---|
| 1-4 | Signetics Part Number, that is, 2600, 2616, 2620, etc. |
| 7-13 | Leave blank _____ Pattern Number to be assigned by Signetics. |
| 15-19 | Punch the letters "CODED" |
| 21 | CS1/$\overline{CS1}$/NC Chip Select Logic Level (If low selects chip, punch "0"; if high selects chip, punch "1"; if no connection, punch "N".) |

## PROGRAMMING INSTRUCTIONS

**2616** (Cont'd)

| | |
|---|---|
| 22 | CS2/$\overline{CS2}$/NC Chip Select Logic Level |
| 23 | CS3/$\overline{CS3}$/NC Chip Select Logic Level |
| 26-78 | Customer Identification |
| 79-80 | ROM Truth Table Number (may be left blank) |

### Comment Cards

Any number of comment cards may be used for specifying the user's name, telephone number, address, any special instructions, etc. On these cards the letter "C" must be punched in column 1 and comments can be punched in columns 2-80.

### Hexadecimal Format Data Cards

| COLUMN | INFORMATION |
|---|---|
| 1-5 | Hexadecimal equivalent of the binary input address ($A_0$ = LSB). This is the initial input address and is punched right justified, that is, 00000, 00020, 00040, etc. |
| 7-8 | Hexadecimal equivalent of the binary output data ($O_0$ = LSB) for initial input address. EXAMPLE: Column 7 is upper 4 bits. |

```
0      0
7----0

10100101

  A    5
  ↑    ↑
Col. 7  Col. 8
```

| | |
|---|---|
| 9-10 | Output data for initial input address +1. |
| 11-12 | Output data for initial input address +2. |
| ⋮ | ⋮ |
| 67-68 | Output data for initial input address +30. |
| 69-70 | Output data for initial input address +31. |
| 79-80 | ROM truth table number (may be left blank) |

### Octal Format Data Cards

| COLUMN | INFORMATION |
|---|---|
| 1-4 | Octal equivalent of the binary input address ($A_0$ = LSB). This is the initial input address and is punched right justified, that is, 0000, 0020, 0040, etc. |
| 5-7 | Octal equivalent of the binary output data ($O_0$ = LSB) for initial input address. EXAMPLE: |

```
0      0
7----0

10100101

2  4  5

Col. 5 ↑      ↑ Col. 7
       ↑
    Col. 6
```

| | |
|---|---|
| 8-10 | Output data for initial input address +1. |
| 11-13 | Output data for initial input address +2. |
| ⋮ | ⋮ |
| 47-49 | Output data for initial input address +14. |
| 50-52 | Output data for initial input address +15. |
| 79-80 | ROM truth table number (may be left blank). |

### Binary Format Data Cards

| COLUMN | INFORMATION |
|---|---|
| 1-5 | Decimal equivalent of the binary input address ($A_0$ = LSB). This is the initial input address and is punched right justified, that is, 00000, 00008, 00016, etc. |
| 7-14 | Binary output data ($O_0$ = LSB) for initial input address. Output data can also be punched with a "P" or an "N" instead of a "1" or a "0," respectively. |

```
0      0
7------0

10100101

Col. 7 ↑      ↑ Col. 14
```

| | |
|---|---|
| 16-23 | Output data for initial input address +1. |
| 25-32 | Output data for initial input address +2. |
| 34-41 | Output data for initial input address +3. |
| 43-50 | Output data for initial input address +4. |
| 52-59 | Output data for initial input address +5. |
| 61-68 | Output data for initial input address +6. |
| 70-77 | Output data for initial input address +7. |
| 79-80 | ROM truth table number (may be left blank). |