PRELIMINARY

5 VOLT BOOT BLOCK FLASH MEMORY

28F002BC (x8)

- **High Performance Read**
  - **80/120 ns Max. Access Time**
    40 ns Max. Output Enable Time
- **Low Power Consumption**
  - **20 mA Typical Read Current**
- **x8-Only Input/Output Architecture**
  - **Space-Constrained 8-bit Applications**
- **Optimized Array Blocking Architecture**
  - **One 16-KB Protected Boot Block**
  - **Two 8-KB Parameter Blocks**
  - **One 96-KB Main Block**
  - **One 128-KB Main Block**
  - **Top Boot Location**
- **Hardware Data Protection Feature**
  - **Erase/Write Lockout during Power Transitions**
  - **Absolute Hardware Protection for Boot Block**
- **Software EEPROM Emulation with Parameter Blocks**
- **Extended Cycling Capability**
  - **100,000 Block Erase Cycles**
- **Automated Byte Write and Block Erase**
- **Industry-Standard Command User Interface**
  - **Status Registers**
  - **Erase Suspend Capability**
- **SRAM-Compatible Write Interface**
- **Reset/Deep Power-Down Input**
  - **0.2 µA I_{CC} Typical**
  - **Provides Reset for Boot Operations**
- **Industry-Standard Surface Mount Packaging**
  - **40-Lead TSOP**
  - **44-Lead PSOP**
  - **40-Lead PDIP**
- **ETOX™ IV Flash Technology**
  - **5 V Read**
- **12 V Write and Block Erase**
  - **V_{PP} = 12 V ±5% Standard**
  - **V_{PP} = 12 V ±10% Option**
- **Independent Software Vendor Support**

The Intel® 2-Mbit flash memory is an extension of the Boot Block architecture which includes block-selective erasure, automated write and erase operations, and a standard microprocessor interface. The 2-Mbit flash memory enhances the Boot Block architecture by adding more density and blocks, x8 input/output control, very high-speed, low-power, and industry-standard ROM-compatible pinout and surface mount packaging.

The Intel® 28F002BC is an 8-bit wide flash memory offering. This high-density flash memory provides user-selectable bus operation for 8-bit applications. The 28F002BC is a 2,097,152-bit nonvolatile memory organized as 262,144 bytes of information. It is offered in 44-lead PSOP, 40-lead PDIP and 40-lead TSOP package, which is ideal for space-constrained portable systems or any application with board space limitations.

This device uses an integrated Command User Interface (CUI) and Write State Machine (WSM) for simplified byte write and block erasure. The 28F002BC provides block locations compatible with the Intel® MCS®-186 family, 80286, 90860CA, and the Intel386™, Intel486™, Pentium®, and Pentium Pro microprocessors.

The boot block includes a data protection feature to protect the boot code in critical applications. With a maximum access time of 80 ns, this high-performance 2-Mbit flash memory interfaces at zero wait-state to a wide range of microprocessors and microcontrollers. A deep power-down mode lowers the total V_{CC} power consumption to 1 µW typical. This power savings is critical in hand-held battery powered systems. For very low-power applications using a 3.3 V supply, refer to the *3 Volt Advanced Boot Block Flash Memory* datasheet (order number 290580). Manufactured on Intel® 0.6 micron ETOX™ IV process technology, the 28F002BC flash memory provides world-class quality, reliability, and cost-effectiveness at the 2-Mbit density.

NOTE: This document formerly known as *28F002BC 2-Mbit (256K x 8) Boot Block Flash Memory*.

December 1998 Order Number: 290578-005

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The 28F002BC may contain design defects or errors known as errata which may cause the product to deviate from published specifications. Current characterized errata are available on request.

Contact your local Intel sales office or your distributor to obtain the latest specifications and before placing your product order.

Copies of documents which have an ordering number and are referenced in this document, or other Intel literature, may be obtained from:

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CONTENTS

PAGE

1.0 INTRODUCTION 5
1.1 Designing for Density Upgradeability 5
1.2 Main Features 5
1.3 Applications 6
1.4 Pinouts 7
1.5 Pin Descriptions 10

2.0 PRODUCT DESCRIPTION 11
2.1 Memory Organization 12
2.1.1 Blocking 12
2.1.2 28F002BC-T Block Memory Map 12

3.0 PRINCIPLES OF OPERATION 12
3.1 Bus Operations 13
3.2 Read Operations 13
3.2.1 Read Array 13
3.2.2 Intelligent Identifiers 14
3.3 Write Operations 14
3.3.1 Command User Interface (CUI) 14
3.3.2 Status Register 17
3.3.3 Program Mode 17
3.3.4 Erase Mode 18
3.3.5 Extended Cycling 19
3.4 Boot Block Locking 19
3.4.1 $V_{PP} = V_{IL}$ for Complete Protection 19
3.4.2 RP# = V_{HH} for Boot Block Unlocking 19

PAGE

3.5 Power Consumption 23
3.5.1 Active Power 23
3.5.2 Standby Power 23
3.5.3 Deep Power-Down 23
3.6 Power-Up/Down Operation 23
3.6.1 RP# Connected to System Reset 23
3.6.2 V_{CC}, V_{PP} and RP# Transitions 23
3.7 Power Supply Decoupling 24
3.7.1 V_{PP} Trace on Printed Circuit Boards 24

4.0 ELECTRICAL SPECIFICATIONS 25
4.1 Absolute Maximum Ratings 25
4.2 Operating Conditions 25
4.3 Capacitance 25
4.4 DC Characteristics 26
4.5 AC Characteristics—Read Only Operations 29
4.6 AC Characteristics—WE#—Controlled Write Operations 30
4.7 AC Characteristics—CE#—Controlled Write Operations 33
4.8 Erase and Program Timings 35

5.0 ORDERING INFORMATION 35

6.0 ADDITIONAL INFORMATION 36

APPENDIX A: WSM Transition Table 37

PRELIMINARY

REVISION HISTORY

Date of Revision	Version	Description
04/01/96	-001	Original version
09/01/96	-002	Pin 2 of 44-Lead PSOP changed from DU to NC Alternate program command (10H) removed WSM transition table added
10/01/96	-003	40-Lead PDIP package added
12/01/97	-004	*Erase Suspend/Resume Flowchart* changed V_{CC} and V_{PP} ranges changed throughout document
12/15/98	-005	Revised Section 1.1, *Designing for Density Upgradeability*, and 1.4, *Pinouts*, to reflect current product offering. Changed document title from *28F002BC 2-Mbit (256K x 8) Boot Block Flash Memory.*

1.0 INTRODUCTION

This datasheet comprises the specifications for the 28F002BC 2-Mbit flash memory. Section 1.0 provides an overview of the 2-Mbit flash memory, including applications, pinouts, and pin descriptions. Section 2.0 describes the memory organization in detail. Section 3.0 defines a description of the memory's principles of operation. Section 4.0 details the memory's operating specifications. Finally, Sections 5.0 and 6.0 provide ordering and reference information.

1.1 Designing for Density Upgradeability

The 28F002BC has been optimized to meet market requirements. Applications currently using the 28F001BX and 28F002BX can migrate to this product. Of course, both the 28F001BX and the 28F002BX devices use an 8-bit wide bus. Those applications needing a 16-bit bus can convert to the 5 Volt Boot Block Flash memory 28F200B5, 28F400B5, 28F800B5 products. Low power applications using a 3.3 V supply can convert to the 3 Volt Advanced Boot Block Flash memory family.

The 28F004B5 product is a natural migration path to the 4-Mbit density. Both the 28F002BC and the 28F004B5 are offered in identical packages to make upgrade seamless. A few simple considerations can smooth the migration path significantly:

1. Connect the NC pin of the 28F002BC to GND (this will retain boot block locking when a 28F004B5 is inserted).

2. Design a switchable V_{PP} to take advantage of the 5 V V_{PP} option on the 28F004B5, device.

3. If anticipating use of the 5 V V_{PP} option, switch V_{PP} to GND for complete write protection.

Previous designs with Intel® 28F002BX devices on occasion had to use a NOR gate (or some other scheme) to prevent issues with floating addresses latching incorrect data. The 28F002BC has corrected this issue and does not need the NOR gate. When migrating a design using the 28F002BX to the 28F002BC, the NOR gate can be removed. When considering upgrading, packaging is of paramount importance. Current and future market trends indicate TSOP and PSOP as the packages that will enable designs into the next century.

1.2 Main Features

The 28F002BC Boot Block flash memory is a high-performance, 2-Mbit (2,097,152 bit) flash memory organized as 256 Kbytes (262,144 bytes) of eight bits each.

The 28F002BC has separately erasable blocks, including a hardware-lockable boot block (16,384 bytes), two parameter blocks (8,192 bytes each) and two main blocks (one block of 98,304 bytes and one block of 131,072 bytes). An erase operation typically erases one of the main blocks in 2.4 seconds and the boot or parameter blocks in 1.0 second. Each block can be independently erased and programmed 100,000 times.

The boot block is located at the top of the address map to match the protocol of many systems, including the Intel® MCS-186 family, 80960CA, i860™ microprocessors as well as Pentium and Pentium Pro microprocessors. The hardware-lockable boot block provides the most secure code storage. The boot block is intended to store the kernel code required for booting-up a system. When the RP# pin is at V_{HH}, the boot block is unlocked and program and erase operations can be performed. When the RP# pin is at V_{PPLK}, the boot block is locked and program and erase operations to the boot block are ignored.

The Command User Interface (CUI) serves as the interface between the microprocessor or microcontroller and the internal operation of the 28F002BC.

Program and Erase Automation allows program and erase operations to be executed using an industry standard two-write command sequence to the CUI. Data writes are performed in byte increments. Each byte in the flash memory can be programmed independently of other memory locations but is erased simultaneously with all other locations within the block.

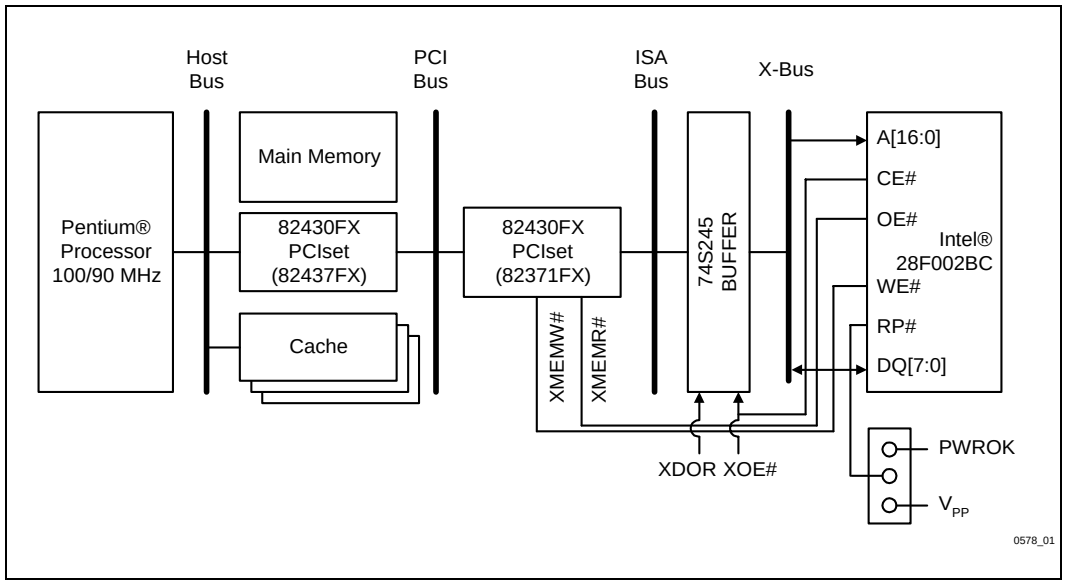


Figure 1. 28F002BC-T Interface to a Pentium® Microprocessor System

The Status Register (SR) indicates the status of the internal Write State Machine (WSM), which reports critical information on program and/or erase sequences.
The maximum access time of 80 ns (t_{ACC}) is guaranteed over the commercial temperature range (0 °C to +70 °C), 10% V_{CC} supply voltage range (4.5 V to 5.5 V) and 100 pF output load. Typical I_{CC} active current is 20 mA.

IPP, the maximum program current, is 20 mA. The standard V_{PP} voltage for erase and program is 11.4 V to 12.6 V (V_{PP} = 12 V ± 5%).

The 28F002BC flash memory is also designed with a standby mode to minimize system current drain and allow for low-power designs. When the CE# and RP# pins are at V_{CC}, the CMOS standby mode is enabled and I_{CC} drops to about 50 µA.

A deep power-down mode is enabled when the RP# pin is at ground. In addition to minimizing power consumption, the deep power-down mode also provides write protection during power-up conditions. I_{CC} current during deep power-down mode is 0.20 µA typical. An initial maximum access time or reset time of 300 ns is required from RP# switching high until outputs are valid. Equivalently, the device has a maximum wake-up time of 215 ns until writes to the CUI are recognized.

When RP# is at ground, the WSM is reset, the status register is cleared, and the entire device is write-protected. This feature prevents data corruption and protects the code stored in the device during system reset. The system Reset pin can be tied to RP# to reset the memory to read mode at power-up. With on-chip program/erase automation and RP# functionality for data protection, the device is protected against unwanted program and/or erase cycles, even during system reset.

1.3 Applications

2-Mbit Boot Block flash memory combines high density, high performance, and cost-effective flash memory with blocking and hardware protection capabilities. Its flexibility and versatility reduces cost throughout the product life cycle. Flash memory is ideal for Just-In-Time production flow, reducing system inventory and costs, and eliminating component handling during the production phase. During a product's life cycle, flash memory reduces costs by allowing user-performed code updates and feature enhancements via floppy disk or remote link.

The 28F002BC is a full-function blocked flash product suitable for a wide range of applications, including extended PC BIOS, digital cellular phone program and data storage, telecommunication boot/firmware, and various embedded applications where both program and data storage are required.

Reprogrammable systems, such as personal computers, are ideal applications for the 28F002BC. Portable and hand-held personal computer applications are becoming more complex with the addition of power management software to take advantage of the latest microprocessor technology, the availability of ROM-based application software, pen tablet code for electronic handwriting, and diagnostic code. Figure 1 shows an example 28F002BC application.

The increase in software sophistication augments the probability that a code update will be required after the PC is shipped. The 28F002BC provides a safe and inexpensive update solution for desktop, notebook, and hand-held personal computers while extending the product lifetime. Furthermore, the deep power-down mode provides added flexibility for those battery-operated portable designs that require low power.

The 28F002BC is also an excellent design solution for analog and digital cellular phone and telecommunication switching applications requiring high-performance, high-density storage in a small form factor package (x8-only bus). The blocking structure allows for easy segmentation of embedded code for modular software designs. For example, the parameter block can be used for frequently updated data storage and diagnostic messages (e.g., phone numbers and authorization codes).

1.4 Pinouts

The 28F002BC in the 44-lead PSOP pinout follows the industry-standard ROM/EPROM pinout, as shown in Figure 4. The 28F200B5 pinout, indicating the WP# input, is also shown in the same diagram. The 40-lead TSOP package (shown in Figure 2) offers the smallest form factor possible. The low-cost 40-lead PDIP package diagram is shown in Figure 3.

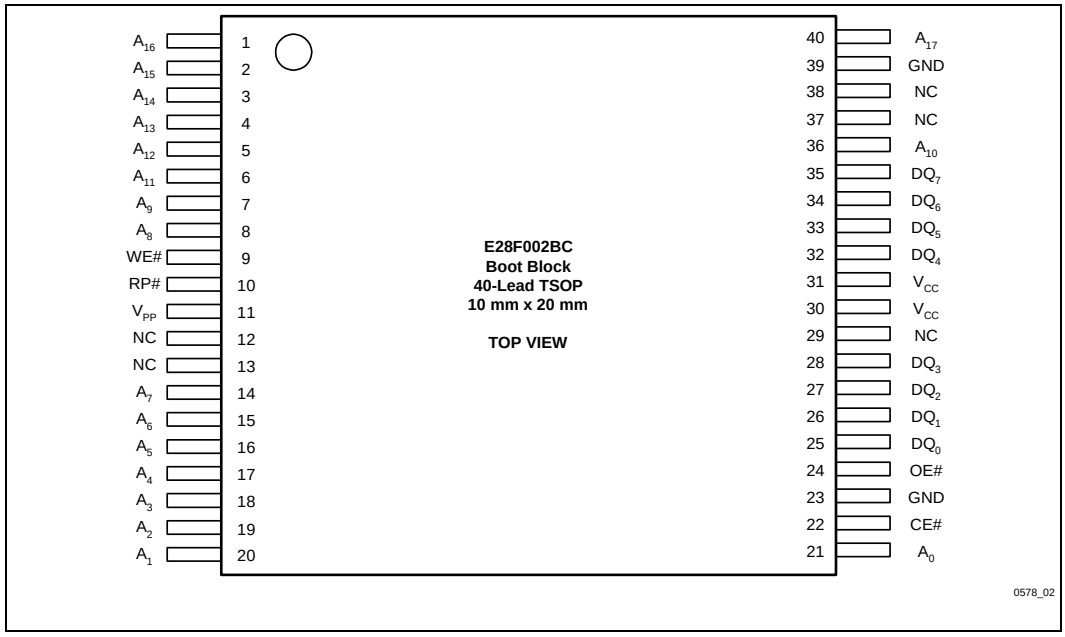


Figure 2. The 40-Lead TSOP Offers the Smallest Form Factor for Space-Constrained Applications

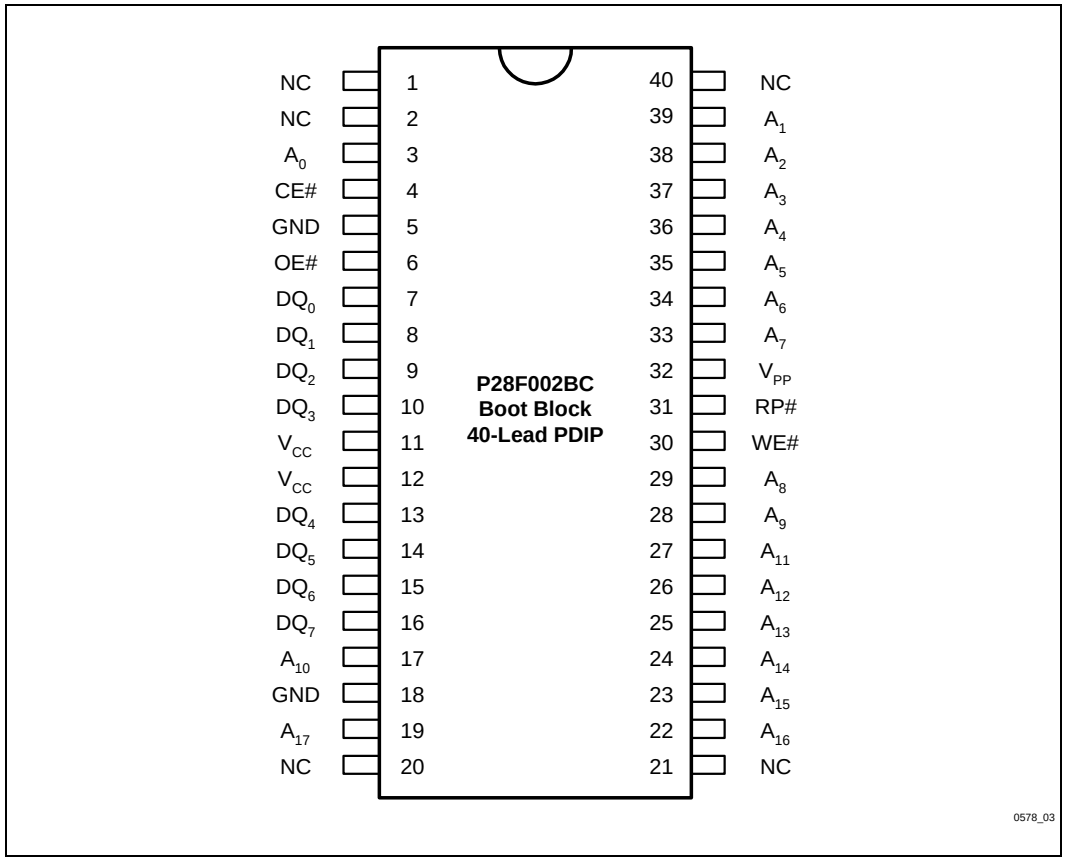


Figure 3. The 40-Lead PDIP Offers the Lowest Cost Package Solution

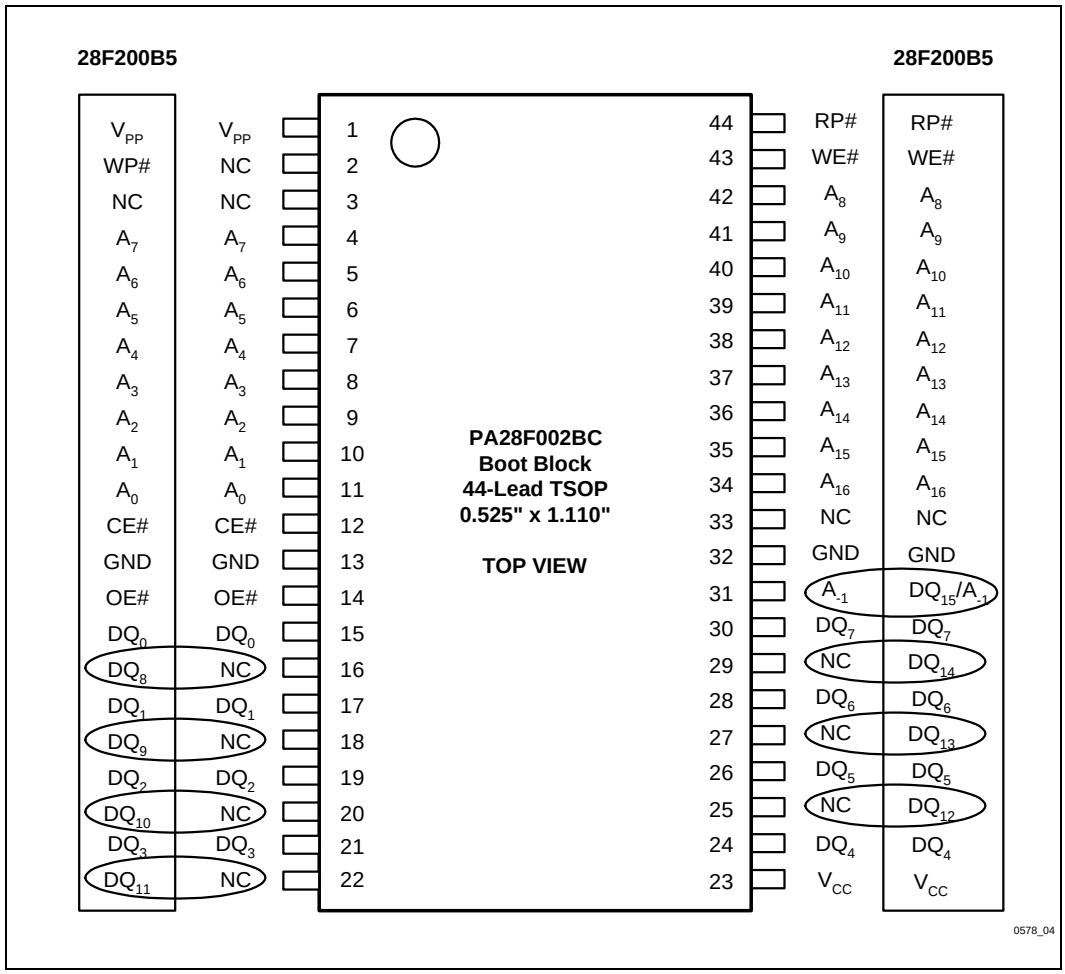


Figure 4. The 44-Lead PSOP Offers a Convenient Upgrade from JEDEC ROM Standards

1.5 Pin Descriptions

Table 1. 28F002BC Pin Descriptions

Symbol	Type	Name and Function
A_{-1}, A_0–A_{17}	INPUT	**ADDRESS INPUTS** for memory addresses. Addresses are internally latched during a write cycle. A_{-1} is used on the PSOP package only. A_{17} is used on the TSOP and PDIP packages.
A_9	INPUT	**ADDRESS INPUT:** When A_9 is at $V_{HH,}$ the signature mode is accessed. During this mode, A_0 decodes between the manufacturer and device IDs.
DQ_0–DQ_7	INPUT/ OUTPUT	**DATA INPUTS/OUTPUTS:** Inputs array data on the second CE# and WE# cycle during a program operation. Inputs commands to the Command User Interface when CE# and WE# are active. Data is internally latched during the write cycle. Outputs array, intelligent identifier and status register data. The data pins float to tri-state when the chip is de-selected or the outputs are disabled.
CE#	INPUT	**CHIP ENABLE:** Activates the device's control logic, input buffers, decoders and sense amplifiers. CE# is active low. CE# high deselects the memory device and reduces power consumption to standby levels. If CE# and RP# are high, but not at a CMOS high level, the standby current will increase due to current flow through the CE# and RP# input stages.
OE#	INPUT	**OUTPUT ENABLE:** Enables the device's outputs through the data buffers during a read cycle. OE# is active low.
WE#	INPUT	**WRITE ENABLE:** Controls writes to the command register and array blocks. WE# is active low. Addresses and data are latched on the rising edge of the WE# pulse.
RP#	INPUT	**RESET/DEEP POWER-DOWN:** Provides three-state control. Puts the device in deep power-down mode, locks, and unlocks the boot block from program/erase. When RP# is at logic high level (6.5 V maximum), the boot block is locked and cannot be programmed or erased. When RP# = V_{HH} (10.8 V minimum), the boot block is unlocked and can be programmed or erased. When RP# is at a logic low level the boot block is locked, the deep power-down mode is enabled and the WSM is reset—preventing any blocks from being programmed or erased. When RP# transitions from logic low to logic high, the flash memory enters the read array mode.
V_{CC}		**DEVICE POWER SUPPLY:** 5.0 V ± 10%, 5.0 V ± 5%
V_{PP}		**PROGRAM/ERASE POWER SUPPLY:** For erasing memory array blocks or programming data in each block. When $V_{PP} < V_{PPLK}$ all blocks are locked and memory contents cannot be altered.
GND		**GROUND:** For all internal circuitry.
NC		**NO CONNECT:** Pin may be driven or left floating.

2.0 PRODUCT DESCRIPTION

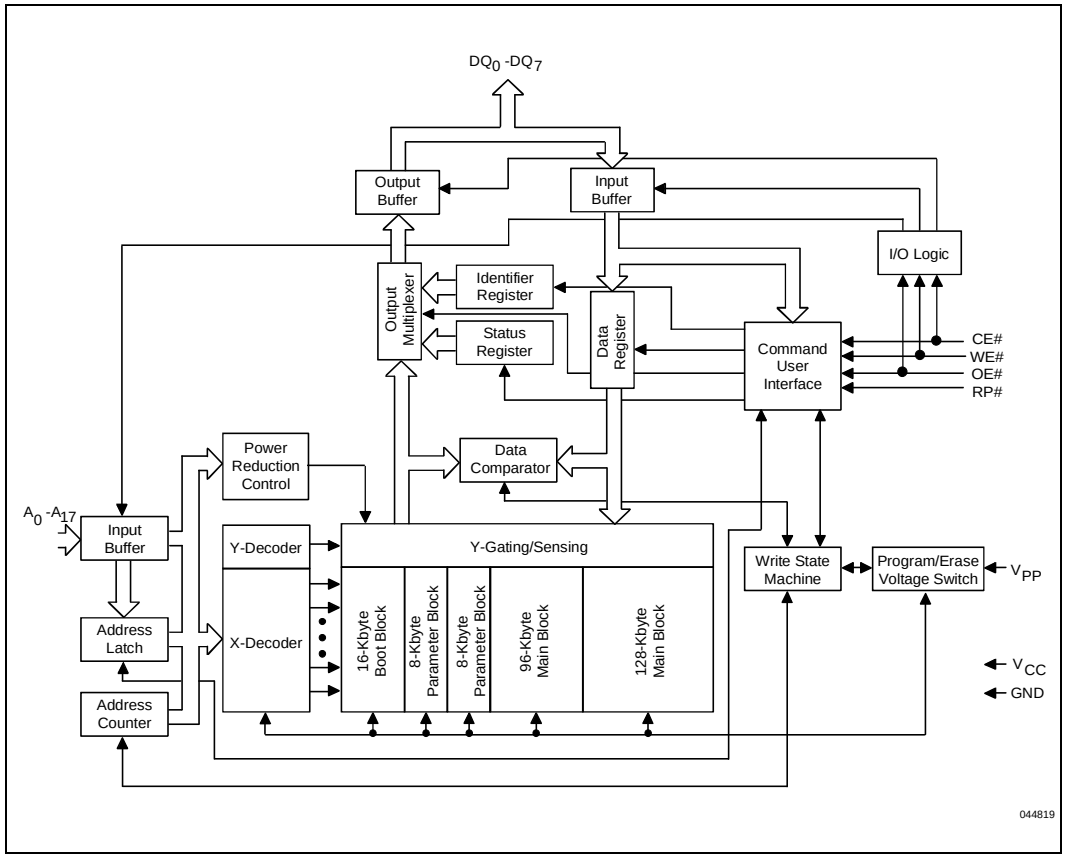


Figure 5. 28F002BC Internal Block Diagram

2.1 Memory Organization

2.1.1 BLOCKING

The 28F002BC features an asymmetrically-blocked architecture that provides system memory integration. Each block can be erased up to 100,000 times. The block sizes have been chosen to optimize their functionality for common applications of nonvolatile storage. For the address locations of the blocks, see the 28F002BC-T Memory Map, Figure 6.

2.1.1.1 Boot Block - 16 KB

The boot block is intended to replace a dedicated boot PROM in a microprocessor or microcontroller-based system. The 16-Kbyte (16,384 bytes) boot block is located at the top of the address map as shown in Figure 6. This boot block features hardware controllable write-protection to protect the crucial microprocessor boot code from accidental erasure. The boot block can be erased and written when RP# is held at 12 V for the duration of the erase or program operation. This feature allows customers to change the boot code when necessary while providing security at other times.

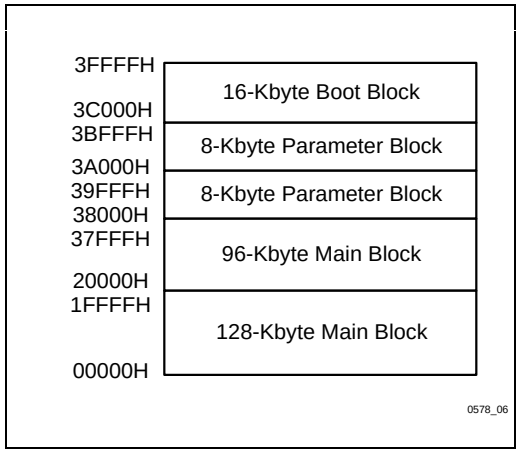


Figure 6. 28F002BC-T Memory Map

2.1.1.2 Parameter Blocks - 8 KB (each)

The 28F002BC has two 8-Kbyte parameter blocks to facilitate storage of frequently updated system parameters that would normally require an EEPROM. The parameter blocks can also be used to store additional boot or main code. By using software techniques, the byte-rewrite functionality of EEPROMs can be emulated. These techniques are detailed in Intel's application note *AP-604 Using Intel's Boot Block Flash Memory Parameter Blocks to Replace EEPROM.*

2.1.1.3 Main Block - 96 KB and 128 KB

The 28F002BC contains one 96-Kbyte (98,304 byte) block and one 128-Kbyte (131,072 byte) block. These blocks are typically used for data or code storage.

2.1.2 28F002BC-T BLOCK MEMORY MAP

The 16-Kbyte boot block of the 28F002BC-T is located from 3C000H to 3FFFFH. The first 8-Kbyte parameter block resides in memory space from 3A000H to 3BFFFH. The second 8-Kbyte parameter block consumes the memory area from 38000H to 39FFFH. The 96-Kbyte main block extends from 20000H to 37FFFH, while the 128-Kbyte main block occupies the region from 00000H to 1FFFFH.

3.0 PRINCIPLES OF OPERATION

Flash memory improves upon EPROM capability with in-circuit electrical write and erase. The Boot Block flash memory utilizes a Command User Interface (CUI) and automated algorithms to simplify write and erase operations. The CUI allows for 100% TTL-level control inputs, fixed power supplies during erasure and programming, and maximum EPROM compatibility.

When $V_{PP} < V_{PPLK}$, the device will only successfully execute the following commands: Read Array, Read Status Register, Clear Status Register, and Intelligent Identifier. The device provides standard EPROM read, standby and output disable operations. Manufacturer identification and device identification data can be accessed through the CUI or through the standard EPROM A_9 high voltage (V_{ID}) access for PROM programming equipment. High voltage on V_{PP} allows write and erase of the device. With V_{PP} active, all functions associated

with altering memory contents are accessible via the CUI.

The purpose of the Write State Machine (WSM) is to automate the write and erasure of the device completely. The WSM will begin operation upon receipt of a signal from the CUI and will report status back through the status register. The CUI will handle the WE# interface to the data and address latches, as well as system software requests for status while the WSM is in operation.

3.1 Bus Operations

Flash memory reads, erases and writes in-system via the local CPU. All bus cycles to or from the flash memory conform to standard microprocessor bus cycles. These bus operations are summarized in Tables 2 and 4.

3.2 Read Operations

The 28F002BC has three user read modes: read array, read intelligent identifier, and read status register.

During power-up conditions, it takes a maximum of 600 ns from when V_{CC} is at 4.5 V to when valid data is available at the outputs.

3.2.1 READ ARRAY

When RP# transitions from V_{IL} (reset) to V_{IH}, the device will be in read array mode and will respond to the read control inputs (CE#, OE#, and address inputs) without any commands being written to the CUI.

When the device is in read array mode, four control signals must be manipulated to read data at the outputs.

- WE# must be logic high (V_{IH})
- CE# must be logic low (V_{IL})
- OE# must be logic low (V_{IL})
- RP# must be logic high (V_{IH})

In addition, the address of the desired location must be applied to the address pins. Refer to *AC Characteristics* for the exact sequence and timing of these signals.

If the device is not in read array mode, as would be the case after a program or erase operation, the Read Mode command (FFH) must be written to the CUI before array reads can take place.

Table 2. 28F002BC Bus Operations

Mode	Notes	RP#	CE#	OE#	WE#	A_9	A_0	V_{PP}	DQ_{0-7}
Read	1,2,3	V_{IH}	V_{IL}	V_{IL}	V_{IH}	X	X	X	D_{OUT}
Output Disable		V_{IH}	V_{IL}	V_{IH}	V_{IH}	X	X	X	High Z
Standby		V_{IH}	V_{IH}	X	X	X	X	X	High Z
Deep Power-Down	8	V_{IL}	X	X	X	X	X	X	High Z
Intelligent Identifier (Mfr)	4	V_{IH}	V_{IL}	V_{IL}	V_{IH}	V_{ID}	V_{IL}	X	89H
Intelligent Identifier (Device)	4	V_{IH}	V_{IL}	V_{IL}	V_{IH}	V_{ID}	V_{IH}	X	7CH
Write	5,6,7	V_{IH}	V_{IL}	V_{IH}	V_{IL}	X	X	V_{PPH}	D_{IN}

NOTES:

1. Refer to *DC Characteristics*.
2. X can be V_{IL}, V_{IH} for control pins and addresses, V_{PPLK} or V_{PPH} for V_{PP}.
3. See *DC Characteristics* for V_{PPLK}, V_{PPH}, V_{HH}, V_{ID} voltages.
4. Manufacturer and device codes may also be accessed via a CUI write sequence, A_1-A_{17} = X.
5. Refer to Table 3 for valid D_{IN} during a write operation.
6. Command writes for program or block erase are only executed when $V_{PP} = V_{PPH}$.
7. To write or erase the boot block, hold RP# at V_{HH}.
8. RP# must be at GND ± 0.2 V to meet the maximum deep power-down current specified.

3.2.2 INTELLIGENT IDENTIFIERS

The manufacturer and device codes are read via the CUI or by taking the A_9 pin to V_{ID}. Writing 90H to the CUI places the device into Intelligent Identifier read mode. A read of location 00000H outputs the manufacturer's identification code, 89H. Reading location 00001H outputs the device ID, 7CH.

The 28F002BC device ID of 7CH is identical to the E28F002BX (40-lead TSOP). It differs from the PA28F200BX (44-lead PSOP), which has a device ID of 2274H. Designers using the PA28F200BX in the x8 mode who wish to migrate to the PA28F002BC need to be mindful of this device ID difference and modify software drivers as necessary. The 40-lead PDIP device ID is 7CH.

3.3 Write Operations

There are two commands that alter memory array contents: Program Setup and Erase Setup/Confirm. In addition, the Erase Suspend command suspends the WSM during an erase operation and releases the CUI to accept any Read command (so long as it is to a block other than the one being erased). Finally, there is a Clear Status Register command for resetting the contents of the status register. This command should be invoked following all operations that modify the status register.

All commands written to the CUI will be interpreted, but for any write operation to be initiated, the V_{PP} voltage must be at V_{HH}. Depending on the application, the design may have a switchable V_{PP} power supply or the V_{PP} may be "hard-wired" to 12 V. The 28F002BC will function normally in either case. It is highly recommended that RP# is tied to the system RESET for data protection during unstable CPU reset and also for proper CPU / flash synchronization.

Furthermore, when attempting to modify the contents of the 28F002BC's boot block area, V_{HH} must be applied to both V_{PP} and RP# for the operation to be valid. Whether attempting to alter the contents of the boot block or any other memory array area, if the proper voltages are not applied to the correct input signals the write operation will be aborted. Subsequently, the status register will respond with either Bit 3 (V_{PP} low error), Bit 4 (program error) or Bit 5 (erase error) being set (refer to Table 5 for status register definitions).

3.3.1 COMMAND USER INTERFACE (CUI)

The Command User Interface (CUI) serves as the interface between the microprocessor and the internal chip controller. Commands are written to the CUI using standard microprocessor write timings. The available commands (summarized in Tables 3 and 4) are Read Array, Read Intelligent Identifier, Read Status Register, Clear Status Register, Program Setup, Erase Setup/Confirm, and Erase Suspend.

For Read commands, the CUI points the read path at either the array, the intelligent identifier, or the status register depending on the command received. For Program or Erase commands, the CUI informs the Write State Machine (WSM) that a Program or Erase has been requested. During the execution of a Program command, the WSM controls the programming sequences and the CUI responds only to status register reads. During an erase cycle, the CUI responds only to status register reads and Erase Suspend. After the WSM has completed its task, it will set the WSM Status bit (bit 7 of the status register) to a "1," which will also allow the CUI to respond to its full command set. Note that after the WSM has returned control to the CUI, the CUI will stay in the read status register mode until it receives another command (see Appendix A).

Table 3. Command Set Codes and Corresponding Device Mode

Command Codes	Device Mode
00	Invalid/Reserved
20	Erase Setup
40	Program Setup
50	Clear Status Register
70	Read Status Register
90	Intelligent Identifier
B0	Erase Suspend
D0	Erase Resume/Erase Confirm
FF	Read Array

Table 4. Command Bus Definitions

Command	Notes	First Bus Cycle			Second Bus Cycle		
		Oper	Addr	Data	Oper	Addr	Data
Read Array		Write	X	FFH			
Intelligent Identifier	1,2	Write	X	90H	Read	IA	IID
Read Status Register		Write	X	70H	Read	X	SRD
Clear Status Register		Write	X	50H			
Program Setup		Write	PA	40H	Write	PA	PD
Block Erase/Confirm		Write	BA	20H	Write	BA	D0H
Erase Suspend/Resume		Write	X	B0H	Write	X	D0H

ADDRESS
BA = Block Address
IA = Identifier Address
PA = Program Address
X = Don't Care

DATA
SRD = Status Register Data
IID = Intelligent Identifier Data
PD = Program Data

NOTES:
1. Bus operations are defined in Table 2.
2. Following the Intelligent Identifier command, two read operations access manufacturer and device codes respectively.

3.3.1.1 Command Function Description

Device operations are selected by writing specific commands into the CUI. Tables 3 and 4 define the available commands. Status register (SR) bits are defined in Table 5.

Invalid/Reserved

These are unassigned commands and should not be used. Intel reserves the right to redefine these codes for future functions.

Read Array (FFH)

This single write cycle command points the read path at the array. If the host CPU performs a CE#/OE#-controlled Read immediately following a two-write sequence (i.e., a Program or Erase command) that started the WSM, then the device will output status register contents. Writing two Read Array (FFH) commands to the CUI aborts the current operation and resets to read array mode.

Executing Read Array after the Erase Setup command (instead of giving Erase Confirm) causes the status register erase and program status bits to be set. This indicates that an erase operation was initiated but not successfully confirmed (an Erase Confirm at this point would be ignored by the CUI). A subsequent Read Array command will point the data path at the array (see Appendix A).

Intelligent Identifier (90H)

After this command is executed, the CUI points the output path to the intelligent identifier circuits. Only intelligent identifier values at addresses 0 and 1 can be read (only address A_0 is used in this mode; all other address inputs are ignored).

Read Status Register (70H)

This is one of three commands that is executable while the WSM is operating. After this command is written, a read of the device will output the contents of the status register, regardless of the address presented to the device. The device automatically enters this mode after program or erase has completed.

Clear Status Register (50H)

The WSM can set the program status and erase status bits in the status register to "1," but it cannot clear them to "0."

The status register is operated in this fashion for two reasons, the first is synchronization. Since the WSM does not know when the host CPU has read the status register, it would not know when to clear the status bits. Second, if the CPU is programming a string of bytes, it may be more efficient to query the status register after programming the string. Thus, if any errors exist while programming the string, the status register will return the accumulated error status. The Clear Status Register command clears the program, erase, and V_{PP} status bits to "0."

Program Setup (40H)

This command simply sets the CUI into a state such that the next write will load the Address and Data registers. After this command is executed, the outputs default to the status register. Two consecutive Read Array commands (FFH) are required to reset to Read Array after the Program Setup command.

Program

The write following the Program Setup command will latch address and data. Also, the CUI initiates the WSM to begin execution of the program algorithm. The device outputs status register data when OE# is enabled**.** To read array data after the program operation is completed, a Read Array command is required.

Erase Setup (20H)

The Erase Setup command prepares the CUI for the Erase Confirm command. No other action is taken. If the next command is not an Erase Confirm command, then the CUI will set both the program status and erase status bits of the status register to a "1," place the device into read status register mode, and wait for another command.

Erase Confirm (D0H)

If the previous command was an Erase Setup command, then the CUI will enable the WSM to erase, at the same time closing the address and data latches, and respond only to the Read Status Register and Erase Suspend commands. While the WSM is executing, the device will output status register data when OE# is toggled low. Status register data can only be updated by toggling either OE# or CE#. If the previous command was not the Erase Setup command (20H), the Erase Confirm command is ignored. Status register bits 4 and 5 are both set to indicate an invalid command sequence.

Erase Suspend (B0H)

This command is only valid while the WSM is executing an erase operation. At all other times, this command is ignored. After this command has been executed, the CUI will set a signal that directs the WSM to suspend erase operations. While waiting for the erase to be suspended, the CUI responds only to the Read Status Register command or to the Erase Resume command. Once the WSM has reached the Suspend state, it will set an output in the CUI that allows the CUI to respond to the Read Array, Read Status Register, and Erase Resume commands. In this mode, the CUI will not respond to any other commands. The WSM will also set the WSM and erase suspend status bits to a "1." The WSM will continue to run, idling in the Suspend state, regardless of the state of all input control pins except V_{PP} and RP#. If V_{PP} is taken below V_{PPLK}, the V_{PP} low status bit (SR.3) will be set and the WSM will abort the suspended erase operation. If active, RP# will immediately shut down the WSM and the remainder of the chip. During a suspend operation, the data and address latches will remain closed, but the address pads are able to drive the address into the read path.

Erase Resume (D0H)

This command will cause the CUI to clear the Suspend state and clear the WSM status bit to a "0," but only if an Erase Suspend command was previously issued. Erase Resume will not have any effect under any other conditions.

3.3.2 STATUS REGISTER

The 28F002BC contains a status register which may be read to determine when a program or erase operation is complete, and whether that operation completed successfully. The status register may be read at any time by writing the Read Status Register command to the CUI. After writing this command, all subsequent read operations output data from the status register until another command is written to the CUI. A Read Array command must be written to the CUI to return to read array mode. The status register bits are output on DQ[0:7]. **The contents of the status register are latched on the falling edge of OE# or CE#, whichever occurs last in the read cycle.** This prevents possible bus errors that might occur if the contents of the status register change while reading the status register. CE# or OE# must be toggled with each subsequent status read to insure the status register is updated; otherwise, the completion of a program or erase operation will not be evident from the status register.

When the WSM is active, the status register will indicate the status of the WSM and upon command completion, it will indicate success or failure of the operation (see Table 5 for definition of status register bits).

3.3.2.1 Clearing the Status Register

The WSM sets status bits "3" through "7" to "1," and clears bits "6" and "7" to "0," but cannot clear status bits "3" through "5" to "0." Bits 3 through 5 can only be cleared by the controlling CPU through the use of the Clear Status Register command. These bits can indicate various error conditions. By allowing the system software to control the resetting of these bits, several operations may be performed (such as cumulatively programming several bytes or erasing multiple blocks in sequence). The status register may then be read to determine if an error occurred during that programming or erasure series. This feature adds flexibility to the way the device may be programmed or erased. To clear the status register, the Clear Status Register command is written to the CUI. Then, any other command may be issued to the CUI. Note, again, that before a read cycle can be initiated, a valid read command must be written to the CUI to specify whether the read data is to come from the memory array, status register, or intelligent identifier.

3.3.3 PROGRAM MODE

Programming is executed using a two-write sequence. The Program Setup command is written to the CUI followed by a second write which specifies the address and data to be programmed. The WSM then executes a sequence of internally-timed events to:

1. Program the desired bits of the addressed memory byte.
2. Verify that the desired bits are sufficiently programmed.

Programming of the memory results in specific bits within a byte being changed to a "0."

If the user attempts to program "1"s, there will be no change in memory contents and no error is reported by the status register.

Similar to erasure, the status register indicates whether programming is complete. While the program sequence is executing, bit 7 of the status register is a "0." The status register can be polled by toggling either CE# or OE# to determine when the program sequence is complete. Only the Read Status Register command is valid while programming is active.

When programming is complete, the status bits, which indicate whether the program operation was successful, should be checked. If the programming operation was unsuccessful, bit 4 of the status register is set to a "1" to indicate a program failure. If bit 3 is set to a "1," then V_{PP} was not within acceptable limits, and the WSM did not execute the programming sequence. If the program operation fails, bit 4 of the status register will be set within 1.5 ms, as determined by the timeout of the WSM.

The status register should be cleared before attempting the next operation. Any CUI instruction can follow after programming is completed; however, reads from the memory array cannot be accomplished until the CUI is given the Read Array command. Figure 7 shows the *Automated Programming Flowchart.*

Table 5. Status Register Bit Definition

WSMS	ESS	ES	DWS	VPPS	R	R	R
7	6	5	4	3	2	1	0

	NOTES:
SR.7 = WRITE STATE MACHINE STATUS (WSMS) 1 = Ready 0 = Busy	The Write State Machine bit must first be checked to determine program or block erase completion, before the program or erase status bits are checked for success.
SR.6 = ERASE-SUSPEND STATUS (ESS) 1 = Erase Suspended 0 = Erase In Progress/Completed	When erase suspend is issued, the WSM halts execution and sets both the WSMS and ESS bits to "1." The ESS bit remains set to "1" until an Erase Resume command is issued.
SR.5 = ERASE STATUS 1 = Error In Block Erasure 0 = Successful Block Erase	When this bit is set to "1," the WSM has applied the maximum number of erase pulses to the block and is still unable to successfully verify block erasure.
SR.4 = PROGRAM STATUS 1 = Error in Byte Program 0 = Successful Byte Program	When this bit is set to "1," the WSM has attempted but failed to program a byte.
SR.3 = V_{PP} STATUS 1 = V_{PP} Low Detect, Operation Abort 0 = V_{PP} OK	The V_{PP} status bit, unlike an A/D converter, does not provide continuous indication of V_{PP} level, but it does check the V_{PP} level intermittently. The WSM interrogates V_{PP} level only after the program or erase command sequences have been entered, and informs the system if V_{PP} has not been switched on. If V_{PP} ever goes below V_{PPLK} (even during an Erase Suspend), the status register will set this bit and abort the operation in progress, even if V_{PP} is returned to a valid level. The V_{PP} status bit is not guaranteed to report accurate feedback between V_{PPLK} and V_{PPH}.
SR.2–SR.0 = RESERVED FOR FUTURE ENHANCEMENTS	These bits are reserved for future use and should be masked out when polling the status register.

3.3.4 ERASE MODE

Erase Setup and Erase Confirm commands to the CUI, along with the address identifying the block to be erased. This address is latched internally when the Erase Confirm command is issued. Block erasure results in all bits within the block being set to "1."

If the Erase Confirm command does not follow the Erase Setup command, the status register responds by setting both SR.4 and SR.5 to "1" to indicate an invalid command sequence. The WSM returns to read status register mode.

The WSM then executes a sequence of internally timed events to:

1. Program all bits within the block to "0."
2. Verify that all bits within the block are sufficiently programmed to "0."
3. Erase all bits within the block (set all bits to "1").
4. Verify that all bits within the block are sufficiently erased.

While the erase sequence is executing, bit 7 of the status register is a "0."

When the status register indicates that erasure is complete, the status bits, which indicate whether the erase operation was successful, should be checked. If the erase operation was unsuccessful, bit 5 of the status register will be set (within 1.5 ms) to "1," indicating an erase failure. If V_{PP} is not within acceptable during the suspended period, the WSM does not execute the erase sequence; instead, bit 5 of the status register is set to a "1" to indicate an erase failure, and bit 3 is set to a "1" to indicate that the V_{PP} supply voltage was outside acceptable limits.

The status register should be cleared before attempting the next operation. Any CUI instruction can follow after erasure is completed; however, reads from the memory array cannot be accomplished until the CUI is given the Read Array command. Figure 8 details the *Automated Block Erase Flowchart.*

3.3.4.1 Suspending and Resuming Erase

Since an erase operation may take a few seconds to complete, an Erase Suspend command is provided. This allows erase-sequence interruption in order to read data from another block of the memory array. Once the erase sequence is started, writing the Erase Suspend command to the CUI requests that the WSM pause the erase sequence at a predetermined point in the erase algorithm. The status register must then be read to determine if the erase operation has been suspended. Taking V_{PP} below V_{PPLK} latches the V_{PP} low status and aborts the operation in progress. V_{PP} should be maintained at valid levels, even during Erase Suspend.

At this point, a Read Array command can be written to the CUI in order to read data from blocks other than that being erased. The only other valid commands at this time are Erase Resume and Read Status Register.

During erase suspend mode, the chip can go into a pseudo-standby mode by taking CE# to V_{IH}, which reduces active current draw.

To resume the erase operation, the chip must be enabled by taking CE# to V_{IL}, then issuing the Erase Resume command. When the Erase Resume command is given, the WSM will continue with the erase sequence and finish erasing the block. As with the end of a standard erase operation, the status register must be read, cleared, and the next instruction issued in order to continue. Figure 9 highlights the *Erase Suspend/Resume Flowchart.*

3.3.5 EXTENDED CYCLING

Intel has designed extended cycling capability into its ETOX IV flash memory technology. The 28F002BC flash memory is designed for 100,000 program/erase cycles on each of the five blocks. At 10% V_{PP}, the parameter blocks are capable of 10,000 program/erase cycles. The combination of low electric fields, clean oxide processing and minimized oxide area per memory cell subjected to the tunneling electric field results in very high cycling capability.

3.4 Boot Block Locking

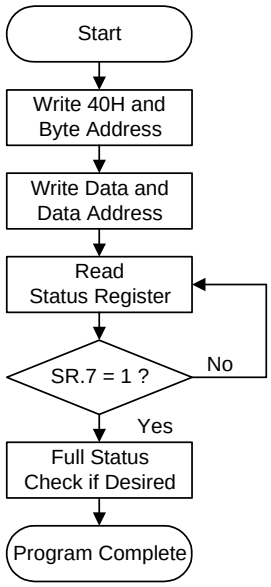
The Boot Block memory architecture features a hardware-lockable boot block so that the kernel code for the system can be kept secure while the parameter and main blocks are programmed and erased independently as necessary. Only the boot block can be locked independently from the other blocks.

3.4.1 $V_{PP} = V_{IL}$ FOR COMPLETE PROTECTION

For complete write protection of all blocks in the flash device, the V_{PP} programming voltage can be held low. When V_{PP} is below V_{PPLK}, any program or erase operation will cause the device to set an error bit in the status register.

3.4.2 RP# = V_{HH} FOR BOOT BLOCK UNLOCKING

In the case of boot block modifications (write and erase), RP# and V_{PP} are set to V_{HH} (12 V). However, if RP# is not at V_{HH} when a program or erase operation of the boot block is attempted, the corresponding status register bit (Bit 4 for Program and Bit 5 for Erase, refer to Table 5 for status register definitions) is set to indicate the failure to complete the specified operation.



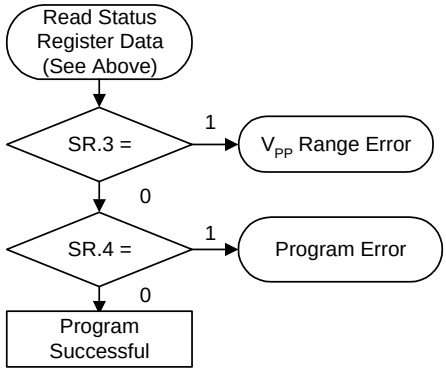
Bus Operation	Command	Comments
Write	Program Setup	Data = 40H Addr = Byte to Program
Write	Program	Data = Data to Program Addr = Location to Program
Read		Status Register Data Toggle CE# or OE# to Update SRD
Standby		Check SR.7 1 = WSM Ready 0 = WSM Busy

Repeat for subsequent writes.

SR Full Status Check can be done after each write, or after a sequence of writes.

Write FFH after the last write operation to reset device to read array mode.

FULL STATUS CHECK PROCEDURE



Bus Operation	Command	Comments
Standby		Check SR.3 1 = V_{PP} Low Detect
Standby		Check SR.4 1 = Program Error

SR.3 **must** be cleared, if set during a program attempt, before further attempts are allowed by the Write State Machine.

SR.4 is only cleared by the Clear Status Register command, in cases where multiple bytes are programmed, before full status is checked.

If an error is detected, clear the status register before attempting retry or other error recovery.

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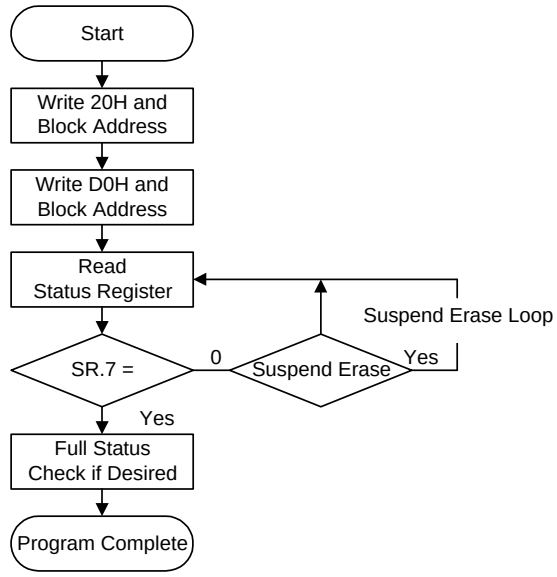
Figure 7. Automated Programming Flowchart



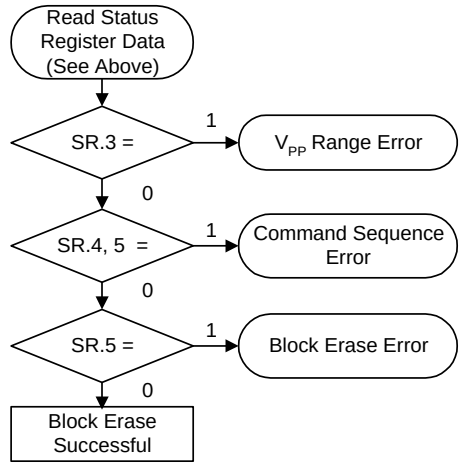
Bus Operation	Command	Comments
Write	Erase Setup	Data = 20H Addr = Within Block to be Erased
Write	Erase Confirm	Data = D0H Addr = Within Block to be Erased
Read		Status Register Data Toggle CE# or OE# to Update SRD
Standby		Check SR.7 1 = WSM Ready 0 = WSM Busy

Repeat for subsequent block erasures.

Full Status Check can be done after each block erase, or after a sequence of block erasures.

Write FFH after the last operation to reset device to read array mode.

FULL STATUS CHECK PROCEDURE



Bus Operation	Command	Comments
Standby		Check SR.3 1 = V_{PP} Low Detect
Standby		Check SR.4, 5 Both 1 = Command Sequence Error
Standby		Check SR.5 1 = Block Erase Error

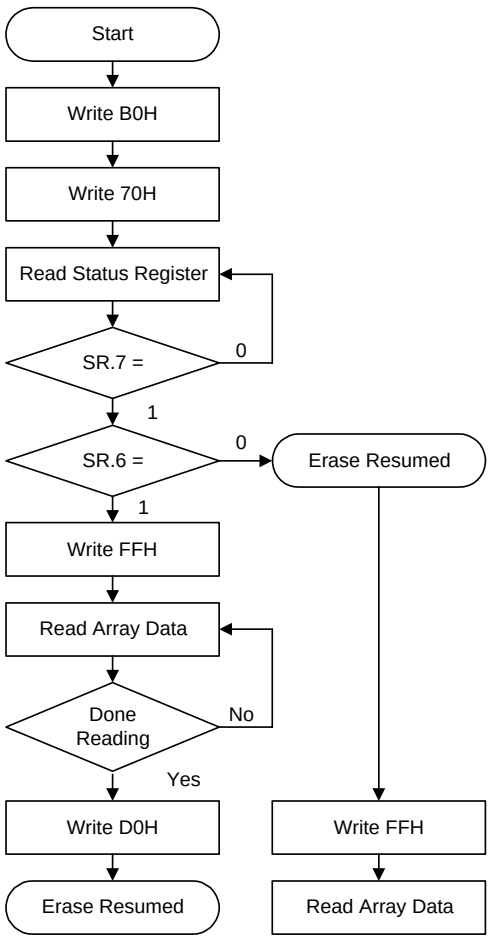
SR.3 **must** be cleared, if set during an erase attempt, before further attempts are allowed by the Write State Machine.

SR.5 is only cleared by the Clear Status Register command, in cases where multiple blocks areeased, before full status is checked.

If an error is detected, clear the status register before attempting retry or other error recovery.

0578_08

Figure 8. Automated Block Erase Flowchart



Bus Operation	Command	Comments
Write	Erase Suspend	Data = B0H Addr = X
Write	Read Status	Data =70H Addr =X
Read		Status Register Data Toggle CE# or OE# to Update Status Register Data Addr = X
Standby		Check SR.7 1 = WSM Ready 0 = WSM Busy
Standby		Check SR.6 1 = Erase Suspended 0 = Erase Completed
Write	Read Array	Data = FFH Addr = X
Read		Read array data from block other than the one being programmed
Write	Erase Resume	Data = D0H Addr = X

Figure 9. Erase Suspend/Resume Flowchart

3.5 Power Consumption

3.5.1 ACTIVE POWER

With CE# at a logic-low level and RP# at a logic-high level, the device is placed in the active mode. The device I_{CC} current is a maximum of 60 mA at 10 MHz with TTL input signals.

3.5.2 STANDBY POWER

With CE# at a logic-high level (V_{IH}), the memory is placed in standby mode, where the maximum I_{CC} standby current is 100 µA. The standby operation disables much of the device's circuitry and substantially reduces device power consumption. The outputs (DQ[0:7]) are placed in a high-impedance state independent of the status of the OE# signal. When CE# is at a logic-high level during erase or program, the device will continue to perform the erase or program function and consume erase or program active power until erase or program is completed.

3.5.3 DEEP POWER-DOWN

The 28F002BC flash memory supports a typical I_{CC} of 0.2 µA in deep power-down mode. This mode is activated by the RP# pin when it is at a logic-low (GND ± 0.2 V); in this mode, all internal circuits are turned off to save power.

Setting the RP# pin low de-selects the memory and places the output drivers in a high impedance state. Recovery from the deep power-down state requires a minimum access time of 300 ns (Section 4.5, *AC Characteristics—Read-Only Operations*, t_{PHQV} parameter).

During erase or program modes, RP# low will abort either erase or program operations, but the memory contents are no longer valid as the data has been corrupted. RP# transitions to V_{IL} or turning power off to the device will clear the status register.

3.6 Power-Up/Down Operation

The 28F002BC offers protection against accidental block erasure or programming during power transitions. **Power supply sequencing is not required**, since the device is indifferent as to which power supply, V_{PP} or V_{CC}, powers-up first. The CUI is reset to the read mode after power-up, but the system must drop CE# low or present a new address to ensure valid data at the outputs.

A system designer must guard against spurious writes when V_{CC} voltages are above V_{LKO} and V_{PP} = V_{HH}. Since both WE# and CE# must be low for a command write, driving either signal to V_{IH} will inhibit writes to the device. The CUI architecture provides additional protection since alteration of memory contents can only occur after successful completion of the two-step command sequences. The device is also disabled until RP# is brought to V_{IH}, regardless of the state of its control inputs. By holding the device in reset (RP# connected to system PowerGood/Reset) during power-up/down, invalid bus conditions during power-up can be masked, providing yet another level of memory protection.

3.6.1 RP# CONNECTED TO SYSTEM RESET

The use of RP# during system reset is important with automated write/erase devices because the system expects to read from the flash memory when it comes out of reset. If a CPU reset occurs without a flash memory reset, proper CPU initialization would not occur because the flash memory may be providing status information instead of array data. Intel's Flash memories allow proper CPU initialization following a system reset by connecting the RP# pin to the same RESET# signal that resets the system CPU.

3.6.2 V_{CC}, V_{PP} AND RP# TRANSITIONS

The CUI latches commands as issued by system software and is not altered by V_{PP}, CE# transitions, or WSM actions. Its default state upon power-up, after exit from deep power-down mode, or after V_{CC} transitions above V_{LKO}, is read array mode.

After any program or block erase operation is complete, and even after V_{PP} transitions down to V_{PPLK}, the CUI must be reset to read array mode via the Read Array command if access to the flash memory is desired.

3.7 Power Supply Decoupling

Flash memory's power switching characteristics require careful device decoupling methods. System designers should consider three supply current issues:

1. Standby current levels (I_{CCS})
2. Active current levels (I_{CCR})
3. Transient peaks produced by falling and rising edges of CE#

Transient current magnitudes depend on the device outputs' capacitive and inductive loading. Two-line control and proper decoupling capacitor selection will suppress these transient voltage peaks. Each flash device should have a 0.1 µF ceramic capacitor connected between each V_{CC} and GND, and between its V_{PP} and GND. These high-frequency, inherently low-inductance capacitors should be placed as close as possible to the package leads.

3.7.1 V_{PP} TRACE ON PRINTED CIRCUIT BOARDS

Designing for in-system writes to the flash memory requires special consideration of the V_{PP} power supply trace by the printed circuit board designer. The V_{PP} pin supplies the flash memory cells current for programming and erasing. One should use similar trace widths and layout considerations given to the V_{CC} power supply trace. Adequate V_{PP} supply traces and decoupling capacitors placed adjacent to the component will decrease spikes and overshoots.

4.0 ELECTRICAL SPECIFICATIONS

4.1 Absolute Maximum Ratings*

Operating Temperature

During Read.....0 °C to +70 °C

During Write and Block Erase ....0 °C to +70 °C

Temperature Bias.....–10 °C to +80 °C

Storage Temperature .....–65 °C to +125 °C

Voltage on Any Pin (except V_{CC}, V_{PP}, A_9 and RP#)

with Respect to GND.....–2.0 V to +7.0 V(1)

Voltage on Pin RP# or Pin A_9

with Respect to GND.....–2.0 V to +13.5 V(1, 2)

V_{PP} Program Voltage

with Respect to GND during Write and Block Erase.....–2.0 V to +14.0 V(1, 2)

V_{CC} Supply Voltage

with Respect to GND.....–2.0 V to +7.0 V(1)

Output Short Circuit Current..... 100 mA(3)

NOTICE: This datasheet contains preliminary information on new products in production. Do not finalize a design with this information. Revised information will be published when the product is available. Verify with your local Intel Sales office that you have the latest datasheet before finalizing a design.

** WARNING: Stressing the device beyond the "Absolute Maximum Ratings" may cause permanent damage. These are stress ratings only. Operation beyond the "Operating Conditions" is not recommended and extended exposure beyond the "Operating Conditions" may effect device reliability.*

NOTES:

1. Minimum DC voltage is -0.5 V on input/output pins. During transitions, this level may undershoot to -2.0 V for periods <20 ns. Maximum DC voltage on input/output pins is V_{CC} + 0.5 V which, during transitions, may overshoot to V_{CC} + 2.0 V for periods <20 ns.
2. Maximum DC voltage on V_{PP} may overshoot to +14.0 V for periods <20 ns. Maximum DC voltage on RP# or A_9 may overshoot to 13.5 V for periods <20 ns.
3. Output shorted for no more than one second. No more than one output shorted at a time.

4.2 Operating Conditions

Table 6. Temperature and V_{CC} Operating Conditions

Symbol	Parameter	Notes	Min	Max	Units
T_A	Operating Temperature		0	70	°C
V_{CC}	5 V V_{CC} Supply Voltage (10%)		4.50	5.50	Volts

4.3 Capacitance

T_A = +25° C, f = 1 MHz

Symbol	Parameter	Notes	Typ	Max	Unit	Conditions
C_{IN}	Input Capacitance	1	6	8	pF	V_{IN} = 0 V
C_{OUT}	Output Capacitance	1, 2	10	12	pF	V_{OUT} = 0 V

NOTES:

1. Sampled, not 100% tested.
2. For the 28F002BC, address pin A_{10} follows the C_{OUT} capacitance numbers.

4.4 DC Characteristics

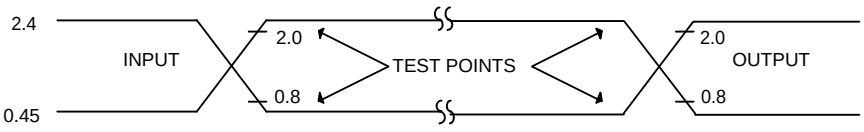
Symbol	Parameter	Notes	Min	Typ	Max	Units	Test Conditions
I_{IL}	Input Load Current	1			± 1.0	µA	$V_{CC} = V_{CC}$ Max $V_{IN} = V_{CC}$ or GND
I_{LO}	Output Leakage Current	1			± 10	µA	$V_{CC} = V_{CC}$ Max $V_{IN} = V_{CC}$ or GND
I_{CCS}	V_{CC} Standby Current	1,3			1.5	mA	$V_{CC} = V_{CC}$ Max CE# = RP# = WP# = V_{IH}
				50	100	µA	$V_{CC} = V_{CC}$ Max CE# = RP# = V_{CC} ± 0.2 V
I_{CCD}	V_{CC} Deep Power-Down Current	1		0.2	8.0	µA	$V_{CC} = V_{CC}$ Max $V_{IN} = V_{CC}$ or GND RP# = GND ± 0.2 V
I_{CCR}	V_{CC} Read Current	1,5		20	55	mA	**CMOS INPUTS** $V_{CC} = V_{CC}$ Max CE# = GND f = 10 MHz I_{OUT} = 0 mA CMOS Inputs: GND ± 0.2 V or V_{CC} ± 0.2 V
				20	60	mA	**TTL INPUTS** $V_{CC} = V_{CC}$ Max CE# = V_{IL} f = 10 MHz I_{OUT} = 0 mA TTL Inputs: V_{IL} or V_{IH}
I_{CCW}	V_{CC} Program Current	1,4			50	mA	Byte Prog. in Progress
I_{CCE}	V_{CC} Erase Current	1,4			30	mA	Block Erase in Progress
I_{CCES}	V_{CC} Erase Suspend Current	1,2		5	10	mA	CE# = V_{IH} Block Erase Suspend
I_{PPS}	V_{PP} Standby Current	1			± 10	µA	$V_{PP} \leq V_{CC}$
I_{PPD}	V_{PP} Deep Power-Down Current	1			5.0	µA	RP# = GND ± 0.2 V
I_{PPR}	V_{PP} Read Current	1			200	µA	$V_{PP} > V_{CC}$
I_{PPW}	V_{PP} Program Current	1,4			20	mA	$V_{PP} = V_{PPH}$ Byte Prog. in Progress
I_{PPE}	V_{PP} Erase Current	1,4			15	mA	$V_{PP} = V_{PPH}$ Block Erase in Progress
I_{PPES}	V_{PP} Erase Suspend Current	1			200	µA	$V_{PP} = V_{PPH}$ Block Erase Suspended

4.4 DC Characteristics (Continued)

Symbol	Parameter	Notes	Min	Typ	Max	Units	Test Conditions
$I_{RP\#}$	RP# Boot Block Unlock Current	1,4			500	µA	RP# = V_{HH}
I_{ID}	A_9 Intelligent Identifier Current	1,4			500	µA	A_9 = V_{ID}
V_{ID}	A_9 Intelligent Identifier Voltage		10.8		13.2	V	
V_{IL}	Input Low Voltage		-0.5		0.8	V	
V_{IH}	Input High Voltage		2.0		V_{CC} + 0.5V	V	
V_{OL}	Output Low Voltage				0.45	V	V_{CC} = V_{CC} Min I_{OL} = 5.8 mA
V_{OH}	Output High Voltage (TTL)		2.4			V	V_{CC} = V_{CC} Min I_{OH} = –2.5 mA
	Output High Voltage (CMOS)		0.85 V_{CC}			V	V_{CC} = V_{CC} Min I_{OH} = –1.5 mA
			V_{CC} – 0.4V				V_{CC} = V_{CC} Min I_{OH} = –100 µA
V_{PPLK}	V_{PP} Lock-Out Voltage	3	0.0		6.5	V	Complete Write Protection
V_{PPH}	V_{PP} (Program/ Erase Operations)	7	11.4	12.0	12.6	V	
V_{PPH}	V_{PP} (Program/ Erase Operations)	8	10.8	12.0	13.2	V	
V_{LKO}	V_{CC} Erase/Write Lock Voltage		2.0			V	
V_{HH}	RP# Unlock Voltage	8	10.8	12.0	13.2	V	Boot Block Unlock Voltage

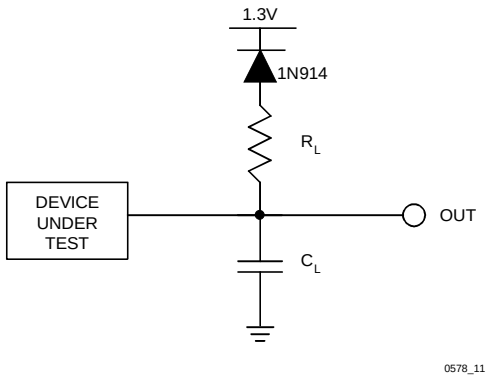
NOTES:

1. All currents are in RMS unless otherwise noted. Typical values at V_{CC} = 5.0 V, V_{PP} =12.0 V , T = +25 °C. These currents are valid for all product versions (packages and speeds).
2. I_{CCES} is specified with the device de-selected. If the device is read while in erase suspend mode, current draw is the sum of I_{CCES} and I_{CCR}.
3. Block erases and byte writes are inhibited when V_{PP} = V_{PPLK}, and not guaranteed in the range between V_{PPH} and V_{PPLK}.
4. Sampled, not 100% tested.
5. CMOS Inputs are either V_{CC} ± 0.2 V or GND ± 0.2 V. TTL Inputs are either V_{IL} or V_{IH}.
6. V_{CC} = 5.0 V ± 10% for applications requiring 100,000 block erase cycles.
7. V_{PP} = 12.0 V ± 5% for applications requiring 100,000 block erase cycles.
8. V_{PP} = 12.0 V ± 10% for applications requiring wider V_{PP} tolerances: Parameter blocks can sustain 10,000 block erase cycles; main blocks support up to 100 block erase cycles. Note that erase times are close to maximum spec limits when using this option.



NOTE:
AC test inputs are driven at V_{OH} (2.4 V_{TTL}) for a logic "1" and V_{OL} (0.45 V_{TTL}) for a logic "0." Input timing begins at V_{IH} (2.0 V_{TTL}) and V_{IL} (0.8 V_{TTL}). Output timing ends at V_{IH} and V_{IL}.

Figure 10. Inputs and Measurement Points



NOTES:
C_L = 100 pF, includes Jig Capacitance
R_L = 3.3KΩ

Figure 11. Standard Test Configuration

4.5 AC Characteristics—Read-Only Operations(1)

Symbol	Parameter	Notes	28F002BC-80		28F002BC-120		Units
			V_{CC} = 5 V ± 10% 100 pF		V_{CC} = 5 V ± 10% 100 pF		
			Min	Max	Min	Max	
t_{AVAV}	Read Cycle Time		80		120		ns
t_{AVQV}	Address to Output Delay			80		120	ns
t_{ELQV}	CE# to Output Delay	2		80		120	ns
t_{PHQV}	RP# to Output Delay			300		300	ns
t_{GLQV}	OE# to Output Delay	2		40		40	ns
t_{ELQX}	CE# to Output in Low Z	3	0		0		ns
t_{EHQZ}	CE# to Output in High Z	3		30		30	ns
t_{GLQX}	OE# to Output in Low Z	3	0		0		ns
t_{GHQZ}	OE# to Output in High Z	3		30		30	ns
t_{OH}	Output Hold from Address, CE#, or OE# Change, Whichever Occurs First	3	0		0		ns

NOTES:

1. See *Inputs and Measurement Points* (Figure 10).
2. OE# may be delayed up to t_{CE}—t_{OE} after the falling edge of CE# without impact on t_{CE}.
3. Sampled, but not 100% tested.
4. See *Standard Test Configuration* (Figure 11).

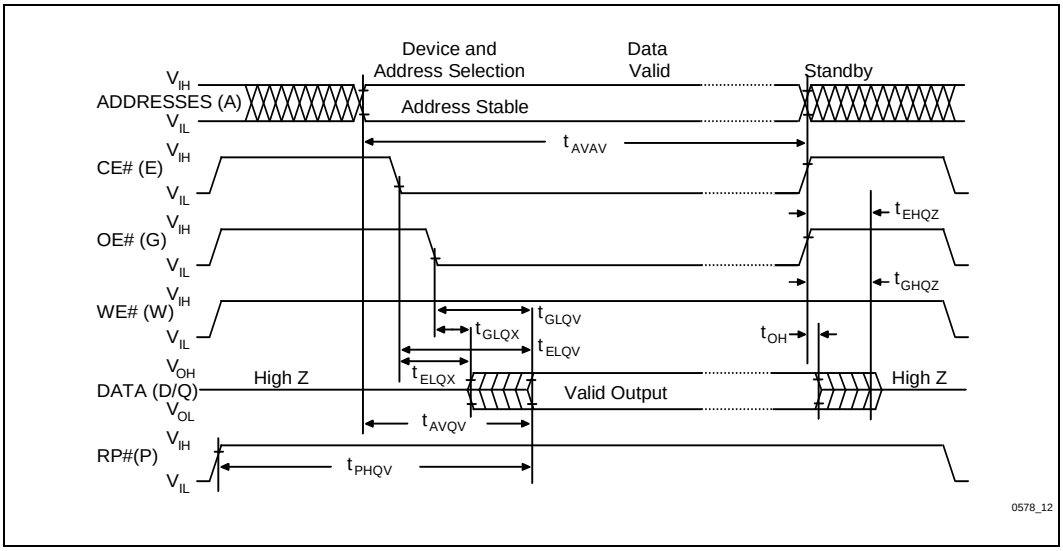


Figure 12. AC Waveforms for Read Operations

4.6 AC Characteristics—WE#-Controlled Write Operations(1)

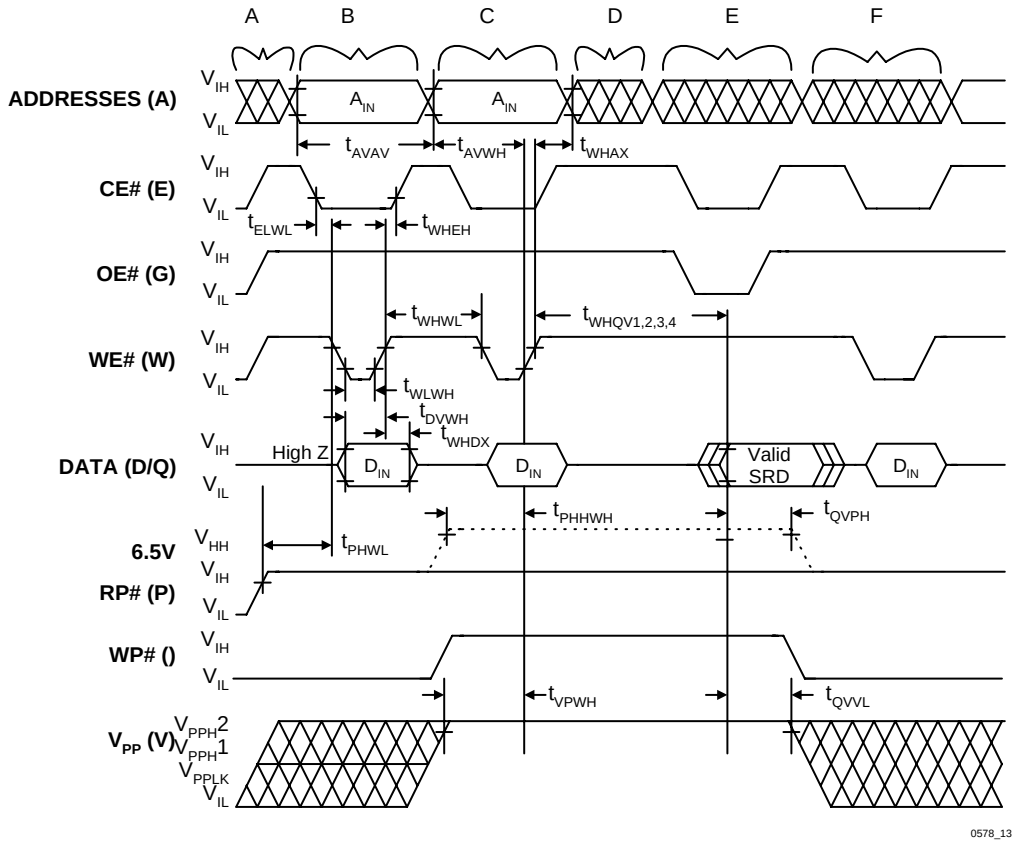
Symbol	Parameter	Notes	28F002BC-80		28F002BC-120		Units
			V_{CC} = 5 V ± 10% 100 pF		V_{CC} = 5 V ± 10% 100 pF		
			Min	Max	Min	Max	
t_{AVAV}	Write Cycle Time		80		120		ns
t_{PHWL}	RP# Setup to WE# Going Low		215		215		ns
t_{ELWL}	CE# Setup to WE# Going Low		0		0		ns
t_{PHHWH}	Boot Block Lock Setup to WE# Going High	6, 8	100		100		ns
t_{VPWH}	V_{PP} Setup to WE# Going High	5, 8	100		100		ns
t_{AVWH}	Address Setup to WE# Going High	3	50		50		ns
t_{DVWH}	Data Setup to WE# Going High	4	50		50		ns
t_{WLWH}	WE# Pulse Width		50		50		ns
t_{WHDX}	Data Hold Time from WE# High	4	0		0		ns
t_{WHAX}	Address Hold Time from WE# High	3	0		0		ns
t_{WHEH}	CE# Hold Time from WE# High		0		0		ns

4.6 AC Characteristics—WE#-Controlled Write Operations[1] (Continued)

Symbol	Parameter	Notes	28F002BC-80		28F002BC-120		Units
			V_{CC} = 5 V ± 10% 100 pF		V_{CC} = 5 V ± 10% 100 pF		
			Min	Max	Min	Max	
t_{WHWL}	WE# Pulse Width High		20		20		ns
t_{WHQV1}	Duration of Programming Operation	2, 5	6		6		µs
t_{WHQV2}	Duration of Erase Operation (Boot)	2, 5, 6	0.3		0.3		s
t_{WHQV3}	Duration of Erase Operation (Parameter)	2,5	0.3		0.3		s
t_{WHQV4}	Duration of Erase Operation (Main)	2, 5	0.6		0.6		s
t_{QVVL}	V_{PP} Hold from Valid SRD	5, 8	0		0		ns
t_{QVPH}	RP# V_{HH} Hold from Valid SRD	6, 8	0		0		ns
t_{PHBR}	Boot Block Lock Delay	7, 8		100		100	ns

NOTES:

1. Read timing characteristics during write and erase operations are the same as during read-only operations. Refer to *AC Characteristics—Read-Only Operations* during read mode.
2. The on-chip WSM completely automates program/erase operations; program/erase algorithms are now controlled internally which includes verify and margining operations.
3. Refer to command definition table for valid A_{IN}.
4. Refer to command definition table for valid D_{IN}.
5. Program/erase durations are measured to valid SRD data (successful operation, SR.7 = 1).
6. For boot block program/erase, RP# should be held at V_{HH} until operation completes successfully.
7. Time t_{PHBR} is required for successful relocking of the boot block.
8. Sampled, but not 100% tested.



NOTES:

A. V_{CC} Power-Up and Standby
B. Write Program Setup or Erase Setup Command
C. Write Valid Address and Data (Program or Erase Confirm Command
D. Automated Program or Erase Delay
E. Read Status Register Data
F. Write Read Array Command

Figure 13. AC Waveforms for Write and Erase Operations (WE#—Controlled Writes)

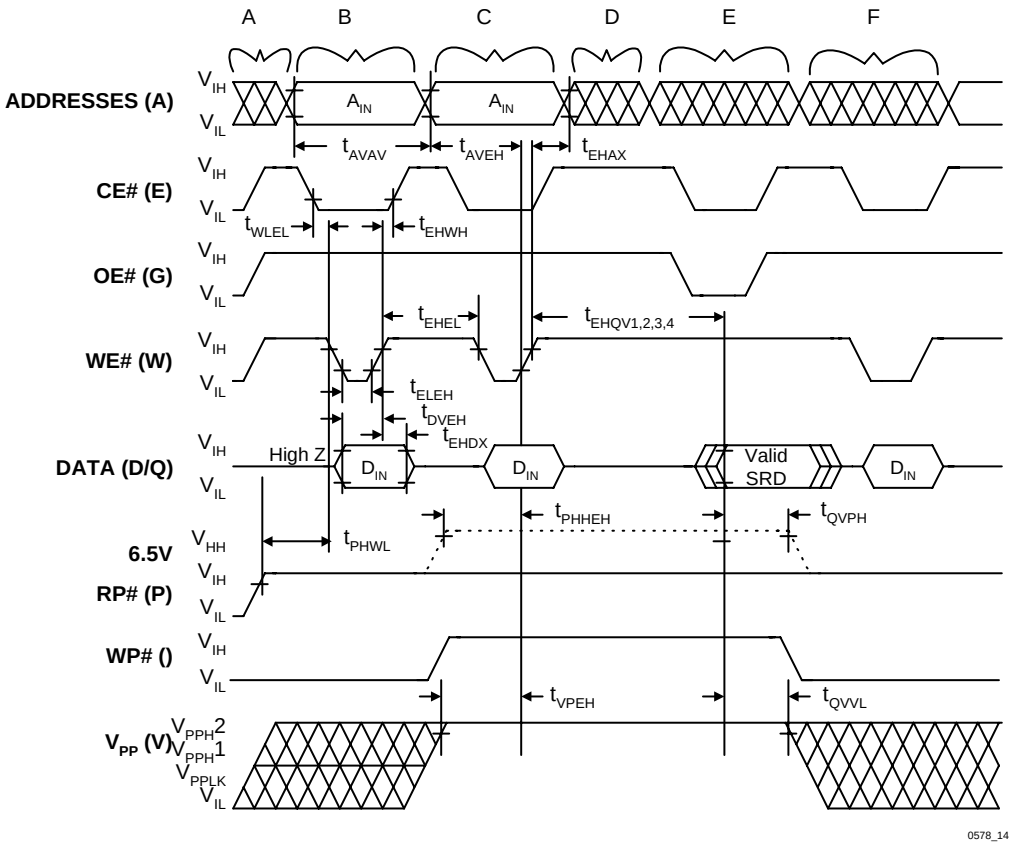
4.7 AC Characteristics—CE#-Controlled Write Operations[1, 9]

Symbol	Parameter	Notes	28F002BC-80		28F002BC-120		Units
			V_{CC} = 5 V ± 10% 100 pF		V_{CC}= 5 V ± 10% 100 pF		
			Min	Max	Min	Max	
t_{AVAV}	Write Cycle Time		80		120		ns
t_{PHEL}	RP# High Recovery to CE# Going Low		215		215		ns
t_{WLEL}	WE# Setup to CE# Going Low		0		0		ns
t_{PHHEH}	Boot Block Lock Setup to CE# Going High	6, 8	100		100		ns
t_{VPEH}	V_{PP} Setup to CE# Going High	5, 8	100		100		ns
t_{AVEH}	Address Setup to CE# Going High	3	50		50		ns
t_{DVEH}	Data Setup to CE# Going High	4	50		50		ns
t_{ELEH}	CE# Pulse Width		50		50		ns
t_{EHDX}	Data Hold Time from CE# High	4	0		0		ns
t_{EHAX}	Address Hold Time from CE# High	3	0		0		ns
t_{EHWH}	WE # Hold Time from CE# High		0		0		ns
t_{EHEL}	CE# Pulse Width High		30		30		ns
t_{EHQV1}	Duration of Programming Operation	2, 5	6		6		µs
t_{EHQV2}	Duration of Erase Operation (Boot)	2, 5, 6	0.3		0.3		s
t_{EHQV3}	Duration of Erase Operation (Parameter)	2, 5	0.3		0.3		s
t_{EHQV4}	Duration of Erase Operation (Main)	2, 5	0.6		0.6		s
t_{QVVL}	V_{PP} Hold from Valid SRD	5, 8	0		0		ns
t_{QVPH}	RP# V_{HH} Hold from Valid SRD	6, 8	0		0		ns
t_{PHBR}	Boot Block Lock Delay	7, 8		100		100	ns

NOTES:

See *AC Characteristics—WE#-Controlled Write Operations* for notes 1 through 8.

9. Chip-Enable controlled writes: write operations are driven by the valid combination of CE# and WE# in systems where CE# defines the write pulse-width (within a longer WE# timing waveform), all set-up, hold and inactive WE# times should be measured relative to the CE# waveform.



NOTES:

A. V_{CC} Power-Up and Standby
B. Write Program Setup or Erase Setup Command
C. Write Valid Address and Data (Program or Erase Confirm Command
D. Automated Program or Erase Delay
E. Read Status Register Data
F. Write Read Array Command

Figure 14. Alternate AC Waveforms for Write and Erase Operations (CE#—Controlled Writes)

4.8 Erase and Program Timings

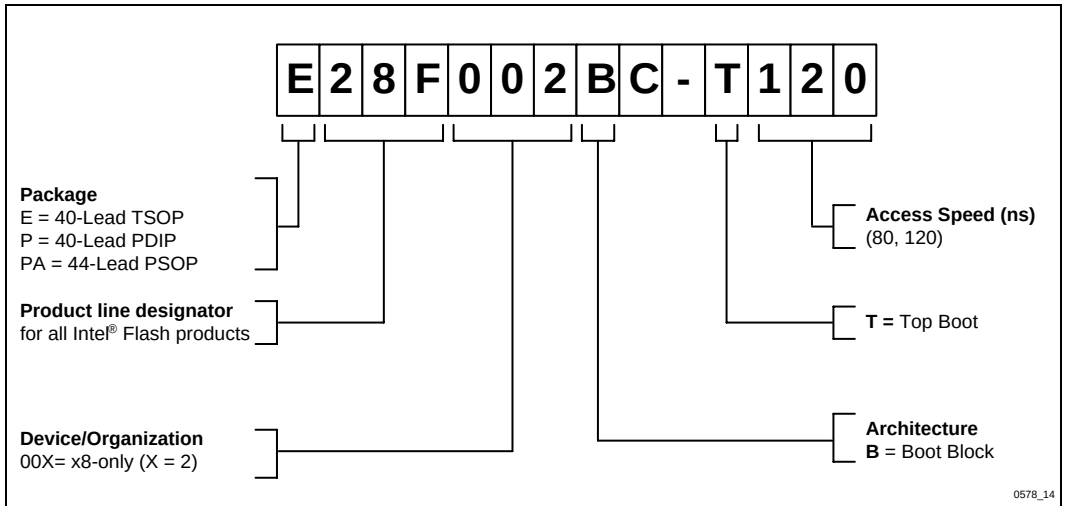
T_A = +25 °C

Parameter(1)	V_{PP} = 12 V ± 10%(2)		V_{PP} = 12 V ± 5%		Units
	V_{CC} = 5 V ± 10%		V_{CC} = 5 V ± 10%		
	Typ	Max	Typ	Max	
Boot/Parameter Block Erase Time	5.8	40	1.0	7	s
Main Block Erase Time	14	60	2.4	14	s
Main Block Write Time	6.0	20	1.2	4.2	s

NOTES:

1. All numbers are sampled, not 100% tested.
2. Erase times near max limits when the 10% V_{PP} option is used.

5.0 ORDERING INFORMATION



VALID COMBINATIONS:

	40-Lead TSOP	40-Lead PDIP	44-Lead PSOP
Commercial 2 M	E28F002BC-T80	P28F002BC-T80	PA28F002BC-T80
	E28F002BC-T120	P28F002BC-T120	PA28F002BC-T120

6.0 ADDITIONAL INFORMATION

Order Number	Document
290580	*3 Volt Advanced Boot Block Flash Memory; 28F004/400B3, 28F008/800B3, 28F016/160B3, 28F320B3* datasheet
292161	*AP-608 Implementing a Plug and Play BIOS Using Intel's Boot Block Flash Memory*
292163	*AP-610 Flash Memory In-System Code and Data Update Techniques*
Note 3	*AB-57 Boot Block Architecture for Safe Firmware Updates*
Note 3	*AP-363 Extended Flash BIOS Concepts for Portable Computers*
Note 3	*AP-604 Using Intel's Boot Block Flash Memory Parameter Blocks to Replace EEPROM*
Note 3	*28F002/200BX-T/B 2-Mbit Boot Block Flash Memory* datasheet
Note 3	*28F004/400BX-T/B 4-Mbit Boot Block Flash Memory* datasheet
Note 3	*28F002/200BV-T/B 2-Mbit SmartVoltage Flash Memory* datasheet
Note 3	*28F004/400BV-T/B 4-Mbit SmartVoltage Flash Memory* datasheet

NOTES:

1. Please call the Intel Literature Center at (800) 548-4725 to request Intel documentation. International customers should contact their local Intel or distribution sales office.
2. Visit Intel's World Wide Web home page at http://www.intel.com for technical documentation and tools.
3. These documents can be located at the Intel World Wide Web support site, http://www.intel.com/support/flash/memory

APPENDIX A
WSM TRANSITION TABLE

Write State Machine Current/Next States

Current State	SR.7	Data When Read	Command Input (and Next State)								
			Read Array (FFH)	Program Setup (40H)	Erase Setup (20H)	Erase Confirm (D0H)	Erase Susp. (B0H)	Erase Resume (D0H)	Read Status (70H)	Clear Status (50H)	Read ID (90H)
Read Array	"1"	Array	Read Array	Program Setup	Erase Setup	Read Array			Read Status	Read Array	Read ID
Program Setup	"1"	Status	Program (Command Input = Byte Program Data)								
Program* (Not Comp.)	"0"	Status	Program								
Program (Comp.)	"1"	Status	Read Array	Program Setup	Erase Setup	Read Array			Read Status	Read Array	Read ID
Erase Setup	"1"	Status	Erase Command Error			Erase	Erase Cmd. Error	Erase	Erase Command Error		
Erase Cmd. Error	"1"	Status	Read Array	Program Setup	Erase Setup	Read Array			Read Status	Read Array	Read ID
Erase (Not Comp.)	"0"	Status	Erase				Erase Susp. to Status	Erase			
Erase (Comp.)	"1"	Status	Read Array	Program Setup	Erase Setup	Read Array			Read Status	Read Array	Read ID
Erase Suspend to Status	"1"	Status	Erase Susp. to Array	Erase Susp. to Array	Erase Susp. to Array	Erase	Erase Susp. to Array	Erase	Erase Susp. to Status	Erase Susp. to Array	Erase Susp. to Array
Erase Suspend to Array	"1"	Array	Erase Susp. to Array	Erase Susp. to Array	Erase Susp. to Array	Erase	Erase Susp. to Array	Erase	Erase Susp. to Status	Erase Susp. to Array	Erase Susp. to Array
Read Status	"1"	Status	Read Array	Program Setup	Erase Setup	Read Array			Read Status	Read Array	Read ID
Read Identifier	"1"	ID	Read Array	Program Setup	Erase Setup	Read Array			Read Status	Read Array	Read ID

NOTE:

You cannot program "1"s to the flash. Writing FFH after the Program Setup command will initiate the program algorithm of the WSM machine. The WSM will attempt the program, realize you are trying to program "1"s, and exit to read status mode without changing memory contents. No error is returned. Writing another FFH while in read status mode will return the flash to Read Array.