# intel® Silicon Gate CMOS 5101, 5101-3, 5101L, 5101L-3

# 1024 BIT (256 x 4) STATIC CMOS RAM

## *Ultra Low Standby Current: 15 nA/Bit for the 5101

- **Fast Access Time—650 ns**
- **Single +5 V Power Supply**
- **$CE_2$ Controls Unconditional Standby Mode**
- **Directly TTL Compatible—All Inputs and Outputs**
- **Three-State Output**

The Intel® 5101 and 5101-3 are ultra-low power 1024 bit (256 words x 4-bits) static RAMs fabricated with an advanced ion-implanted silicon gate CMOS technology. The devices have two chip enable inputs. When $CE_2$ is at a low level, the minimum standby current is drawn by these devices, regardless of any other input transitions on the addresses and other control inputs. Also, when $\overline{CE_1}$ is at a high level and address and other control transitions are inhibited, the minimum standby current is drawn by these devices. When in standby the 5101 and 5101-3 draw from the single 5 volt supply only 15 microamps and 200 microamps, respectively. These devices are ideally suited for low power applications where battery operation or battery backup for non-volatility are required.

The 5101 and 5101-3 use fully DC stable (static) circuitry; it is not necessary to pulse chip select for each address transition. The data is read out non-destructively and has the same polarity as the input data. All inputs and outputs are directly TTL compatible. The 5101 and 5101-3 have separate data input and data output terminals. An output disable function is provided so that the data inputs and outputs may be wire OR-ed for use in common data I/O systems.

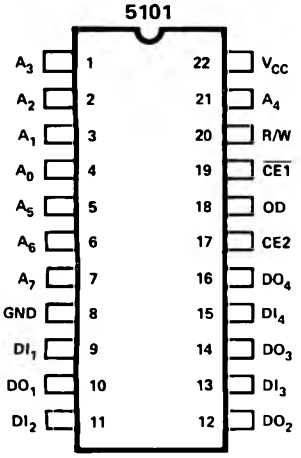
*The 5101L and 5101L-3 are identical to the 5101 and 5101-3, respectively, with the additional feature of guaranteed data retention at a power supply voltage as low as 2.0 volts.*

A pin compatible N-channel static RAM, the Intel 2101, is also available for low cost applications where a 256 x 4 organization is needed.

The Intel ion-implanted, silicon gate, complementary MOS (CMOS) allows the design and production of ultra-low power, high performance memories.

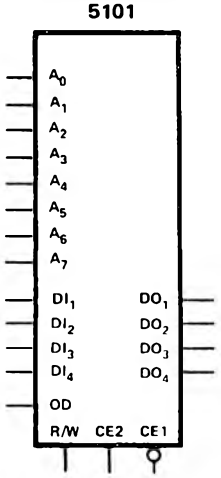
### PIN CONFIGURATION

5101




### LOGIC SYMBOL

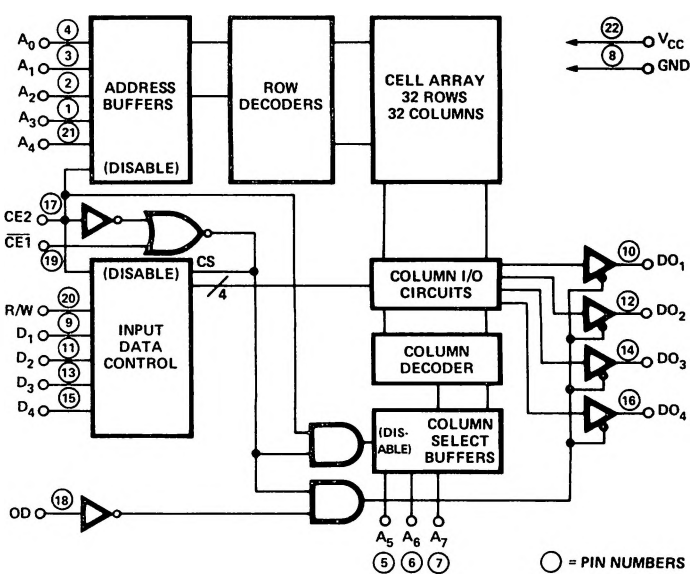
5101




### PIN NAMES

| | | | |
|---|---|---|---|
| $DI_1 - DI_4$ | DATA INPUT | OD | OUTPUT DISABLE |
| $A_0 - A_7$ | ADDRESS INPUTS | $DO_1 - DO_4$ | DATA OUTPUT |
| R/W | READ/WRITE INPUT | $V_{CC}$ | POWER (+5V) |
| $\overline{CE1}$, CE2 | CHIP ENABLE | | |

### BLOCK DIAGRAM



## Absolute Maximum Ratings *

Ambient Temperature Under Bias . . . . . 0°C to 70°C
Storage Temperature . . . . . -65°C to +150°C
Voltage On Any Pin
With Respect to Ground . . . . -0.3V to $V_{CC}$ +0.3V
Maximum Power Supply Voltage . . . . . +7.0V
Power Dissipation . . . . . 1 Watt

*COMMENT:

*Stresses above those listed under "Absolute Maximum Rating" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or at any other condition above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.*

## D. C. and Operating Characteristics for 5101, 5101-3, 5101L, 5101L-3

$T_A$ = 0°C to 70°C, $V_{CC}$ = 5V ±5% unless otherwise specified.

| Symbol | Parameter | Min. | Typ.[1] | Max. | Unit | Test Conditions |
|---|---|---|---|---|---|---|
| $I_{LI}$[2] | Input Current | | 5 | | nA | $V_{IN}$ = 0 to 5.25V |
| $I_{LOH}$[2] | Output High Leakage | | | 1 | μA | $\overline{CE1}$ = 2.2V, $V_{OUT}$ = $V_{CC}$ |
| $I_{LOL}$[2] | Output Low Leakage | | | 1 | μA | $\overline{CE1}$ = 2.2V, $V_{OUT}$ = 0.0V |
| $I_{CC1}$ | Operating Current | | 9 | 22 | mA | $V_{IN}$ = $V_{CC}$ Except $\overline{CE1}$ ≤0.01V Outputs Open |
| $I_{CC2}$ | Operating Current | | 13 | 27 | mA | $V_{IN}$ = 2.2V Except $\overline{CE1}$ ≤0.65V Outputs Open |
| 5101 $I_{CCL}$[2] | Standby Current | | | 15 | μA | $V_{IN}$ = 0 to $V_{CC}$, Except CE2 ≤ 0.2V |
| 5101-3 $I_{CCL}$[2] | Standby Current | | | 200 | μA | $V_{IN}$ = 0 to $V_{CC}$, Except CE2 ≤ 0.2V |
| $V_{IL}$ | Input "Low" Voltage | -0.3 | | 0.65 | V | |
| $V_{IH}$ | Input "High" Voltage | 2.2 | | $V_{CC}$ | V | |
| $V_{OL}$ | Output "Low" Voltage | | | 0.4 | V | $I_{OL}$ = 2.0mA |
| $V_{OH}$ | Output "High" Voltage | 2.4 | | | V | $I_{OH}$ = 1.0mA |

### Low $V_{CC}$ Data Retention Characteristics (For 5101L and 5101L-3) $T_A$ = 0°C to 70°C

| Symbol | Parameter | Min. | Typ.[1] | Max. | Unit | Test Conditions | |
|---|---|---|---|---|---|---|---|
| $V_{DR}$ | $V_{CC}$ for Data Retention | 2.0 | | | V | CE2 ≤ 0.2V | |
| 5101L $I_{CCDR}$ | Data Retention Current | | | 15 | μA | | $V_{DR}$ = 2.0V |
| 5101L-3 $I_{CCDR}$ | Data Retention Current | | | 200 | μA | | $V_{DR}$ = 2.0V |
| $t_{CDR}$ | Chip Deselect to Data Retention Time | 0 | | | ns | | |
| $t_R$ | Operation Recovery Time | $t_{RC}$[3] | | | ns | | |

NOTES: 1. Typical values are $T_A$ = 25°C and nominal supply voltage. 2. Current through all inputs and outputs included in $I_{CCL}$ measurement. 3. $t_{RC}$ = Read Cycle Time.

# A.C. Characteristics for 5101, 5101-3, 5101L, 5101L-3

**READ CYCLE** $T_A$ = 0°C to 70°C, $V_{CC}$ = 5V ±5%, unless otherwise specified.

| Symbol | Parameter | Min. | Typ. | Max. | Unit | Test Conditions |
|---|---|---|---|---|---|---|
| $t_{RC}$ | Read Cycle | 650 | | | ns | (See below) |
| $t_A$ | Access Time | | | 650 | ns | |
| $t_{CO1}$ | Chip Enable ($\overline{CE1}$) to Output | | | 600 | ns | |
| $t_{CO2}$ | Chip Enable (CE2) to Output | | | 700 | ns | |
| $t_{OD}$ | Output Disable To Output | | | 350 | ns | |
| $t_{DF}$ | Data Output to High Z State | 0 | | 150 | ns | |
| $t_{OH1}$ | Previous Read Data Valid with Respect to Address Change | 0 | | | ns | |
| $t_{OH2}$ | Previous Read Data Valid with Respect to Chip Enable | 0 | | | ns | |

**WRITE CYCLE**

| Symbol | Parameter | Min. | Typ. | Max. | Unit | Test Conditions |
|---|---|---|---|---|---|---|
| $t_{WC}$ | Write Cycle | 650 | | | ns | (See below) |
| $t_{AW}$ | Write Delay | 150 | | | ns | |
| $t_{CW1}$ | Chip Enable ($\overline{CE1}$) To Write | 550 | | | ns | |
| $t_{CW2}$ | Chip Enable (CE2) To Write | 550 | | | ns | |
| $t_{DW}$ | Data Setup | 400 | | | ns | |
| $t_{DH}$ | Data Hold | 100 | | | ns | |
| $t_{WP}$ | Write Pulse | 400 | | | ns | |
| $t_{WR}$ | Write Recovery | 50 | | | ns | |
| $t_{DS}$ | Output Disable Setup | 150 | | | ns | |

### A. C. CONDITIONS OF TEST

Input Pulse Levels: +0.65 Volt to 2.2 Volt

Input Pulse Rise and Fall Times: 20nsec

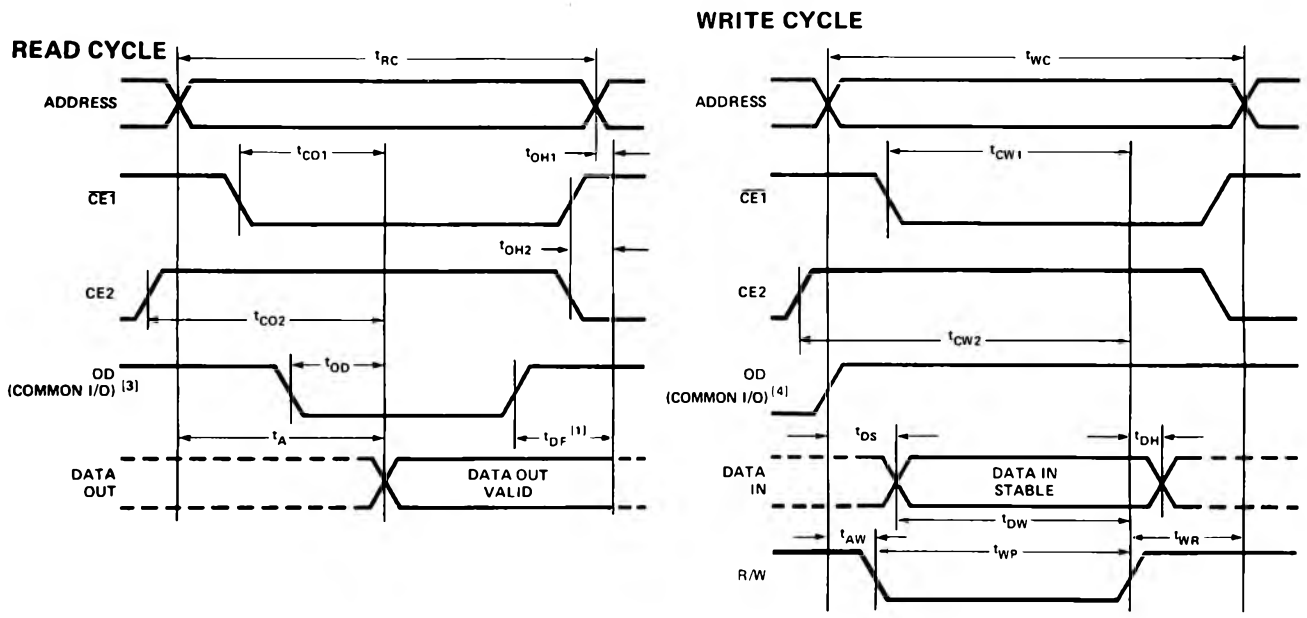
Timing Measurement Reference Level: 1.5 Volt

Output Load: 1 TTL Gate and $C_L$ = 100pF

### Capacitance[2] $T_A$ = 25°C, f = 1MHz

| Symbol | Test | Limits (pF) | |
|---|---|---|---|
| | | Typ. | Max. |
| $C_{IN}$ | Input Capacitance (All Input Pins) $V_{IN}$ = 0V | 4 | 8 |
| $C_{OUT}$ | Output Capacitance $V_{OUT}$ = 0V | 8 | 12 |

# Waveforms




NOTES:
1. Typical values are for $T_A$ = 25°C and nominal supply voltage.
2. This parameter is periodically sampled and is not 100% tested.
3. OD may be tied low for separate I/O operation.
4. During the write cycle, OD is "high" for common I/O and "don't care" for separate I/O operation.

## Low $V_{CC}$ Data Retention