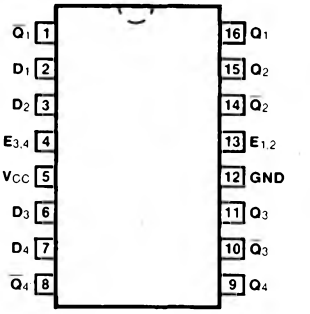
54/7475

4-BIT BISTABLE LATCH

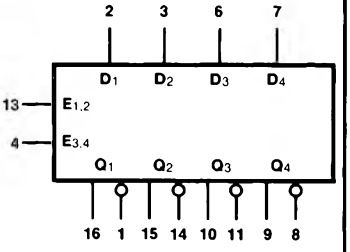
CONNECTION DIAGRAM
PINOUT A



DESCRIPTION — The '75 latch is used as temporary storage for binary information between processing units and input/output or indicator units. Information present at a data (D) input is transferred to the Q output when the Enable is HIGH and the Q output will follow the data input as long as the Enable remains HIGH. When the Enable goes LOW, the information (that was present at the data input at the time the transition occurred) is retained at the Q output until the Enable is permitted to go HIGH.

The '75 features complementary Q and $\overline{Q}$ output from a 4-bit latch and is available in 16-pin packages. For higher component density applications, the '77 4-bit latch is available in the 14-pin package with $\overline{Q}$ outputs omitted.

LOGIC SYMBOL



V_{CC} = Pin 5
GND = Pin 12

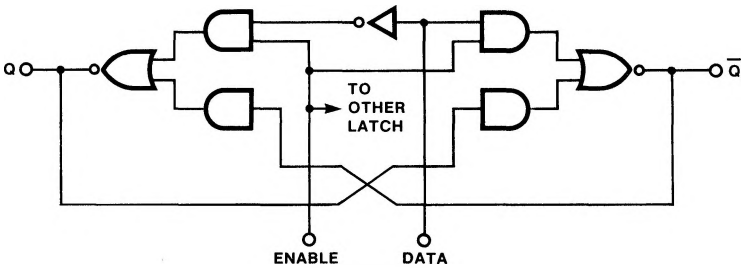
ORDERING CODE: See Section 9

PKGS	PIN OUT	COMMERCIAL GRADE V_{CC} = +5.0 V ±5%, T_A = 0°C to +70°C	MILITARY GRADE V_{CC} = +5.0 V ±10%, T_A = -55°C to +125°C	PKG TYPE
Plastic DIP (P)	A	7475PC		9B
Ceramic DIP (D)	A	7475DC	5475DM	6B
Flatpak (F)	A	7475FC	5475FM	4L

INPUT LOADING/FAN-OUT: See Section 3 for U.L. definitions

PIN NAMES	DESCRIPTION	54/74 (U.L.) HIGH/LOW
D_1 — D_4	Data Inputs	2.0/2.0
$E_{1,2}$	Enable Input, Latches 1, 2	4.0/4.0
$E_{2,3}$	Enable Input, Latches 3, 4	4.0/4.0
Q_1 — Q_4	Latch Outputs	10/10
$\overline{Q}_1$ — $\overline{Q}_4$	Complementary Latch Outputs	10/10

LOGIC DIAGRAM



TRUTH TABLE
(Each Latch)

INPUT	OUTPUT
@ t_n	@ t_{n+1}
D	Q
H	H
L	L

NOTES:
t_n = bit time before enable negative-going transition.
t_{n+1} = bit time after enable negative-going transition.
H = HIGH Voltage Level
L = LOW Voltage Level

DC CHARACTERISTICS OVER OPERATING TEMPERATURE RANGE (unless otherwise specified)

SYMBOL	PARAMETER		54/74 Min	54/74 Max	UNITS	CONDITIONS
I_{CC}	Power Supply Current	XM		46	mA	V_{CC} = Max, All Inputs = Gnd
		XC		53		

AC CHARACTERISTICS: V_{CC} = +5.0 V, T_A = +25°C (See Section 3 for waveforms and load configurations)

SYMBOL	PARAMETER	54/74 C_L = 15 pF R_L = 400 Ω Min	54/74 C_L = 15 pF R_L = 400 Ω Max	UNITS	CONDITIONS
t_{PLH} t_{PHL}	Propagation Delay D to Q		30 25	ns	Figs. 3-1, 3-5
t_{PLH} t_{PHL}	Propagation Delay D to $\overline{Q}$		40 15	ns	Figs. 3-1, 3-4
t_{PLH} t_{PHL}	Propagation Delay E to Q, $\overline{Q}$		30 15	ns	Figs. 3-1, 3-8

AC OPERATING REQUIREMENTS: V_{CC} = +5.0 V, T_A = +25°C

SYMBOL	PARAMETER	54/74 Min	54/74 Max	UNITS	CONDITIONS
t_s (H)	Setup Time HIGH, D to E	20		ns	Fig. 3-14
t_h (H)	Hold Time HIGH, D to E	0		ns	Fig. 3-14
t_s (L)	Setup Time LOW, D to E	20		ns	Fig. 3-14
t_h (L)	Hold Time LOW, D to E	0		ns	Fig. 3-14
t_w (H)	E Pulse Width HIGH	20		ns	Fig. 3-8