

# 54ACQ646,54ACTQ646

*54ACTQ646 Quiet Series Octal Transceiver/Register with 3-STATE Outputs*



Literature Number: SNOS135

## 54ACTQ646 Quiet Series Octal Transceiver/Register with 3-STATE Outputs

### General Description

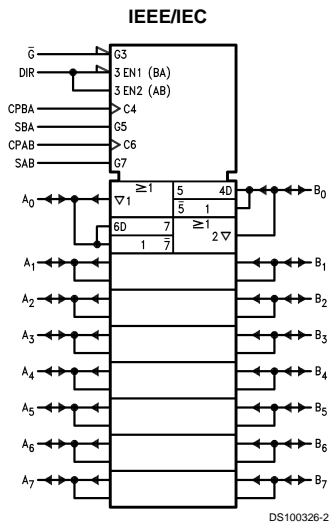
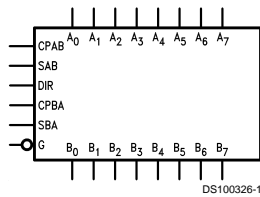
The ACTQ646 consist of registered bus transceiver circuits, with outputs, D-type flip-flops, and control circuitry providing multiplexed transmission of data directly from the input bus or from the internal storage registers. Data on the A or B bus will be loaded into the respective registers on the LOW-to-HIGH transition of the appropriate clock pin (CPAB or CPBA). The four fundamental handling functions available are illustrated in *Figures 1, 2, 3, 4*.

The ACTQ utilizes FSC Quiet Series technology to guarantee quiet output switching and improved dynamic threshold performance. FACT Quiet Series™ features GTO™ output control and undershoot corrector in addition to a split ground bus for superior performance.

### Features

- Guaranteed simultaneous switching noise level and dynamic threshold performance
- Independent registers for A and B busses
- Multiplexed real-time and stored data transfers
- 300 mil slim dual-in-line package
- Outputs source/sink 24 mA
- Faster prop delays than the standard AC/ACT646
- 4 kV minimum ESD immunity
- Standard Microcircuit Drawing (SMD) 5962-9219601

### Logic Symbols



### Pin Descriptions

Pin Names	Description
A <sub>0</sub> -A <sub>7</sub>	Data Register A Inputs Data Register A Outputs
B <sub>0</sub> -B <sub>7</sub>	Data Register B Inputs Data Register B Outputs
CPAB, CPBA	Clock Pulse Inputs
SAB, SBA	Transmit/Receive Inputs

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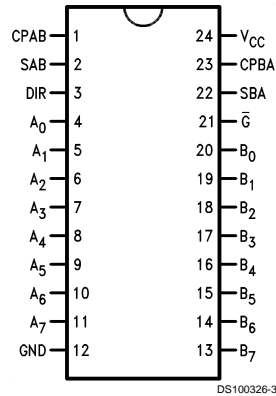
## Logic Symbols (Continued)

## Pin Descriptions (Continued)

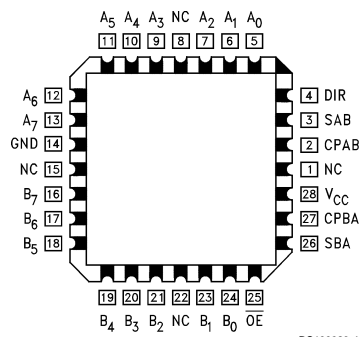
Pin Names	Description
$\overline{G}$	Output Enable Input
DIR	Direction Control Input

## Connection Diagram

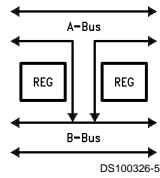
Pin Assignment  
for DIP and Flatpack



Pin Assignment  
for LCC

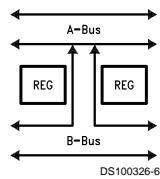


**Real Time Transfer  
A-Bus to B-Bus**



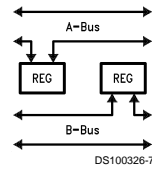
**FIGURE 1.**

**Real Time Transfer  
B-Bus to A-Bus**



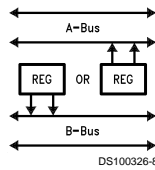
**FIGURE 2.**

**Storage from  
Bus to Register**



**FIGURE 3.**

**Transfer from  
Register to Bus**



**FIGURE 4.**

## Function Table

Inputs						Data I/O (Note 1)		Function
$\bar{G}$	DIR	CPAB	CPBA	SAB	SBA	A <sub>0</sub> -A <sub>7</sub>	B <sub>0</sub> -B <sub>7</sub>	
H	X	H or L	H or L	X	X	Input	Input	Isolation Clock A <sub>n</sub> Data into A Register Clock B <sub>n</sub> Data into B Register
L	H	X	X	L	X	Input	Output	A <sub>n</sub> to B <sub>n</sub> — Real Time (Transparent Mode) Clock A <sub>n</sub> Data into A Register A Register to B <sub>n</sub> (Stored Mode) Clock A <sub>n</sub> Data into A Register and Output to B <sub>n</sub>
L	H	N	X	L	X			
L	H	H or L	X	H	X			
L	H	N	X	H	X			
L	L	X	X	X	L	Output	Input	B <sub>n</sub> to A <sub>n</sub> — Real Time (Transparent Mode) Clock B <sub>n</sub> Data into B Register B Register to A <sub>n</sub> (Stored Mode) Clock B <sub>n</sub> Data into B Register and Output to A <sub>n</sub>
L	L	X	N	X	L			
L	L	X	H or L	X	H			
L	L	X	N	X	H			

H = HIGH Voltage Level

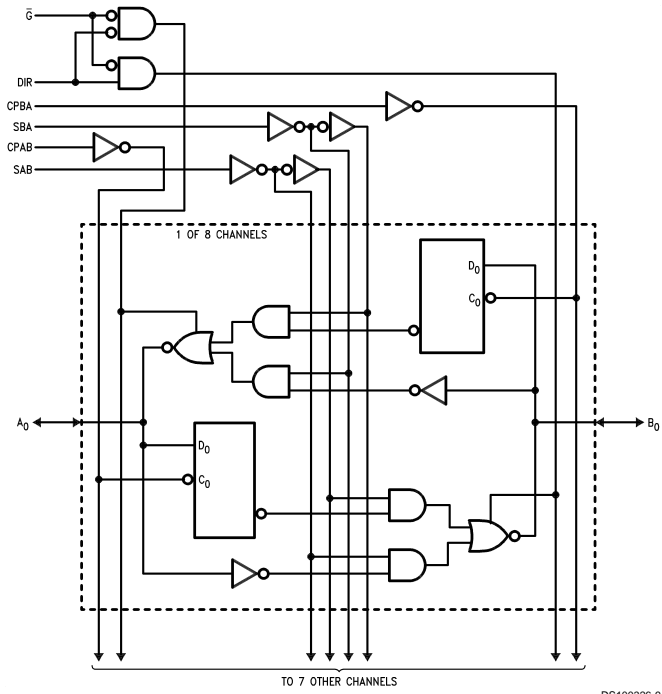
L = LOW Voltage Level

X = Immaterial

N = LOW-to-HIGH Transition

**Note 1:** The data output functions may be enabled or disabled by various signals at the  $\bar{G}$  and DIR inputs. Data input functions are always enabled; i.e., data at the bus pins will be stored on every LOW-to-HIGH transition of the appropriate clock inputs.

## Logic Diagram



DS100326-9

Please note that this diagram is provided only for the understanding of logic operations and should not be used to estimate propagation delays.

## Absolute Maximum Ratings (Note 2)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Supply Voltage ( $V_{CC}$ )	-0.5V to +7.0V
DC Input Diode Current ( $I_{IK}$ )	
$V_I = -0.5V$	-20 mA
$V_I = V_{CC} + 0.5V$	+20 mA
DC Input Voltage ( $V_I$ )	-0.5V to $V_{CC} + 0.5V$
DC Output Diode Current ( $I_{OK}$ )	
$V_O = -0.5V$	-20 mA
$V_O = V_{CC} + 0.5V$	+20 mA
DC Output Voltage ( $V_O$ )	-0.5V to $V_{CC} + 0.5V$
DC Output Source	
or Sink Current ( $I_O$ )	±50 mA
DC $V_{CC}$ or Ground Current	
per Output Pin ( $I_{CC}$ or $I_{GND}$ )	±50 mA
Storage Temperature ( $T_{STG}$ )	-65°C to +150°C
DC Latch-Up Source	
or Sink Current	±300 mA

Junction Temperature ( $T_J$ )

CDIP

175°C

## Recommended Operating Conditions

Supply Voltage ( $V_{CC}$ )	ACTQ	4.5V to 5.5V
Input Voltage ( $V_I$ )		0V to $V_{CC}$
Output Voltage ( $V_O$ )		0V to $V_{CC}$
Operating Temperature ( $T_A$ )	54ACTQ	-55°C to +125°C
Minimum Input Edge Rate $\Delta V/\Delta t$	ACTQ Devices	
	$V_{IN}$ from 0.8V to 2.0V	
	$V_{CC}$ @ 4.5V, 5.5V	125 mV/ns

**Note 2:** Absolute maximum ratings are those values beyond which damage to the device may occur. The databook specifications should be met, without exception, to ensure that the system design is reliable over its power supply, temperature, and output/input loading variables. Fairchild does not recommend operation of FACT™ circuits outside databook specifications.

## DC Electrical Characteristics for ACTQ

Symbol	Parameter	$V_{CC}$ (V)	$T_A =$ -55°C to +125°C		Units	Conditions	
			Guaranteed Limits				
$V_{IH}$	Minimum High Level Input Voltage	4.5	2.0	2.0	V	$V_{OUT} = 0.1V$ or $V_{CC} - 0.1V$	
		5.5	2.0	2.0			
$V_{IL}$	Maximum Low Level Input Voltage	4.5	0.8	0.8	V	$V_{OUT} = 0.1V$ or $V_{CC} - 0.1V$	
		5.5	0.8	0.8			
$V_{OH}$	Minimum High Level Output Voltage	4.5	4.4	4.4	V	$I_{OUT} = -50 \mu A$	
		5.5	5.4	5.4			
			4.5	3.7	3.7	V	(Note 3) $V_{IN} = V_{IL}$ or $V_{IH}$ $I_{OH} = -24 mA$ $I_{OH} = -24 mA$
			5.5	4.7	4.7		
$V_{OL}$	Maximum Low Level Output Voltage	4.5	0.1	0.1	V	$I_{OUT} = 50 \mu A$	
		5.5	0.1	0.1			
			4.5	0.5	0.5	V	(Note 3) $V_{IN} = V_{IL}$ or $V_{IH}$ $I_{OL} = 24 mA$ $I_{OL} = 24 mA$
			5.5	0.5	0.5		
$I_{IN}$	Maximum Input Leakage Current	5.5	±1.0		μA	$V_I = V_{CC}, GND$	
$I_{OZT}$	Maximum I/O Leakage Current ( $A_n, B_n$ Inputs)	5.5	±10.0		μA	$V_I = V_{IL}, V_{IH}$ $V_O = V_{CC}, GND$	
$I_{CCT}$	Maximum $I_{CC}$ /Input	5.5	1.6		mA	$V_I = V_{CC} - 2.1V$	
$I_{OLD}$	(Note 4) Minimum Dynamic	5.5	50		mA	$V_{OLD} = 1.65V$ Max	
$I_{OHD}$	Output Current	5.5	-50		mA	$V_{OHD} = 3.85V$ Min	
$I_{CC}$	Maximum Quiescent Supply Current	5.5	160.0		μA	$V_{IN} = V_{CC}$ or GND (Note 5)	

## DC Electrical Characteristics for ACTQ (Continued)

Symbol	Parameter	V <sub>CC</sub> (V)	T <sub>A</sub> = -55°C to +125°C		Units	Conditions
			Guaranteed Limits			
V <sub>OLP</sub>	Quiet Output Maximum Dynamic V <sub>OL</sub>	5.0	1.5		V	(Note 6)
V <sub>OLV</sub>	Quiet Output Minimum Dynamic V <sub>OL</sub>	5.0	-1.2		V	(Note 6)

**Note 3:** All outputs loaded; thresholds on input associated with output under test.

**Note 4:** Maximum test duration 2.0 ms, one output loaded at a time.

**Note 5:** I<sub>CC</sub> for 54ACTQ @ 25°C is identical to 74ACTQ @ 25°C.

**Note 6:** Max number of outputs defined as (n). Data inputs are driven 0V to 3V. One output @ GND.

## AC Electrical Characteristics

Symbol	Parameter	V <sub>CC</sub> (V) (Note 7)	T <sub>A</sub> = -55°C to +125°C C <sub>L</sub> = 50 pF		Units
			Min	Max	
t <sub>PLH</sub> , t <sub>PHL</sub>	Propagation Delay Clock to Bus	5.0	2.0	11.0	ns
t <sub>PLH</sub> , t <sub>PHL</sub>	Propagation Delay Bus to Bus	5.0	2.0	12.0	ns
t <sub>PLH</sub> , t <sub>PHL</sub>	Propagation Delay SBA or SAB to A <sub>n</sub> or B <sub>n</sub> (w/A <sub>n</sub> or B <sub>n</sub> HIGH or LOW)	5.0	2.0	12.5	ns
t <sub>PZH</sub> , t <sub>PZL</sub>	Enable Time $\bar{G}$ to A <sub>n</sub> or B <sub>n</sub>	5.0	1.5	15.0	ns
t <sub>PHZ</sub> , t <sub>PLZ</sub>	Disable Time $\bar{G}$ to A <sub>n</sub> or B <sub>n</sub>	5.0	1.5	12.0	ns
t <sub>PZH</sub> , t <sub>PZL</sub>	Enable Time DIR to A <sub>n</sub> or B <sub>n</sub>	5.0	1.5	15.0	ns
t <sub>PHZ</sub> , t <sub>PLZ</sub>	Disable Time DIR to A <sub>n</sub> or B <sub>n</sub>	5.0	1.5	12.0	ns

**Note 7:** Voltage Range 5.0 is 5.0V ±0.5V

## AC Operating Requirements

Symbol	Parameter	V <sub>CC</sub> (V) (Note 8)	T <sub>A</sub> = -55°C to +125°C C <sub>L</sub> = 50 pF		Units
			Guaranteed Minimum		
t <sub>S</sub>	Setup Time, HIGH or LOW Bus to Clock	5.0	3.0		ns
t <sub>H</sub>	Hold Time, HIGH or LOW Bus to Clock	5.0	1.5		ns
t <sub>W</sub>	Clock Pulse Width HIGH or LOW	5.0	4.0		ns

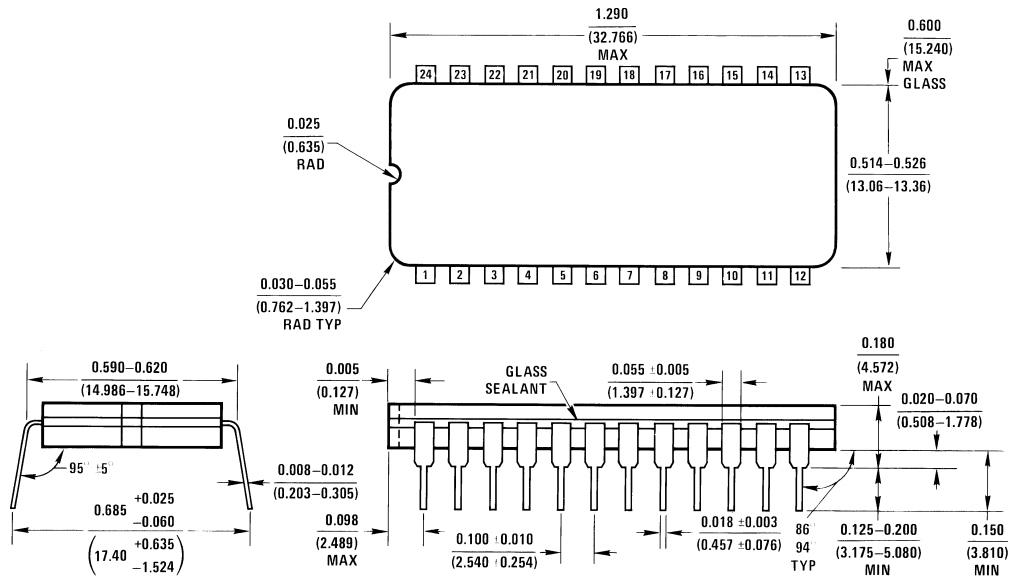
**Note 8:** Voltage Range 5.0 is 5.0V ±0.5V

## Capacitance

Symbol	Parameter	Max	Units	Conditions
C <sub>IN</sub>	Input Capacitance	15	pF	V <sub>CC</sub> = OPEN
C <sub>I/O</sub>	Input/Output Capacitance	20.0	pF	V <sub>CC</sub> = 5.0V
C <sub>PD</sub>	Power Dissipation Capacitance	100.0	pF	V <sub>CC</sub> = 5.0V

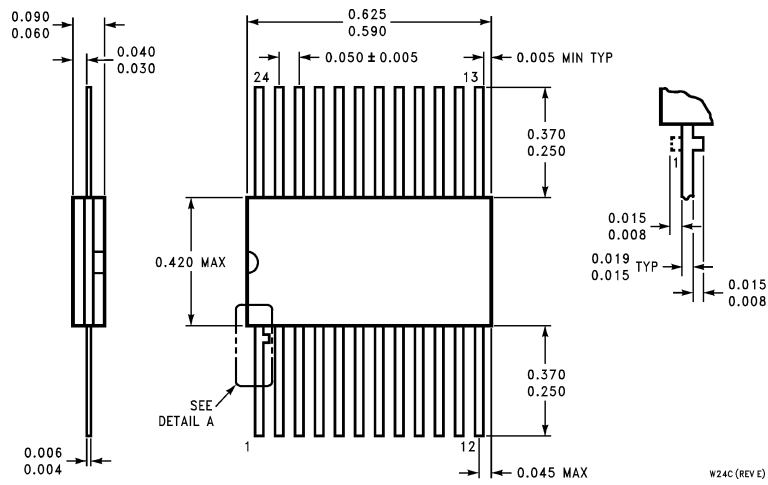


**Physical Dimensions** inches (millimeters) unless otherwise noted



J24A (REV H)

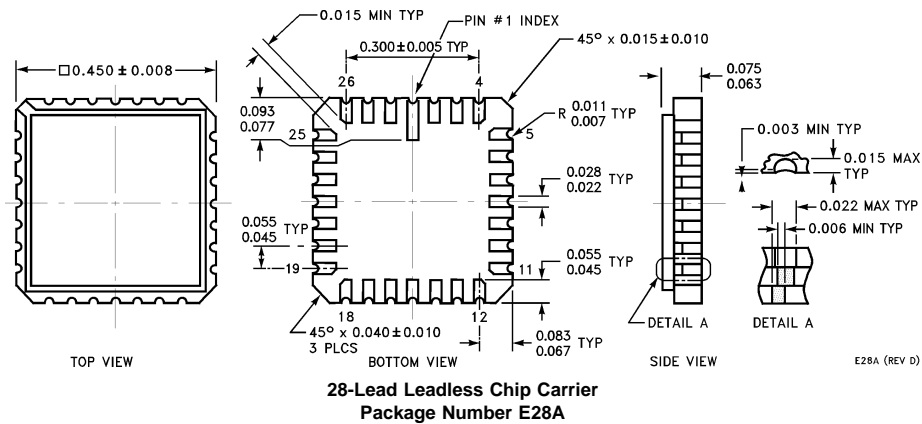
**24-Lead Ceramic Dual-In-Line**  
**Package Number J24A**



W24C (REV E)

**24-Lead Cerpack**  
**Package Number W24C**

**Physical Dimensions** inches (millimeters) unless otherwise noted (Continued)



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