

## 54AC299 • 54ACT299

### 8-Input Universal Shift/Storage Register with Common Parallel I/O Pins

#### General Description

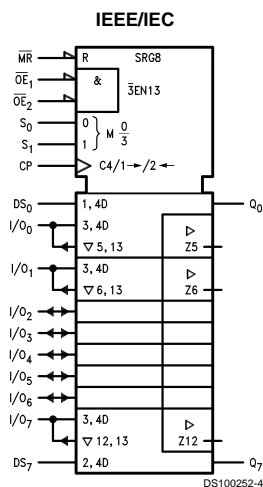
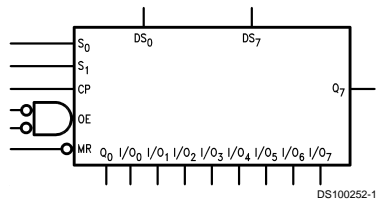
The 'AC/'ACT299 is an 8-bit universal shift/storage register with TRI-STATE® outputs. Four modes of operation are possible: hold (store), shift left, shift right and load data. The parallel load inputs and flip-flop outputs are multiplexed to reduce the total number of package pins. Additional outputs are provided for flip-flops Q<sub>0</sub>, Q<sub>7</sub> to allow easy serial cascading. A separate active LOW Master Reset is used to reset the register.

- Common parallel I/O for reduced pin count
- Additional serial inputs and outputs for expansion
- Four operating modes: shift left, shift right, load and store
- TRI-STATE outputs for bus-oriented applications
- Outputs source/sink 24 mA
- 'ACT299 has TTL-compatible inputs
- Standard Microcircuit Drawing (SMD)
  - 'AC299: 5962-88754
  - 'ACT299: 5962-88771

#### Features

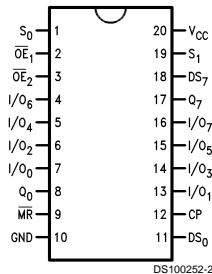
- I<sub>CC</sub> and I<sub>OZ</sub> reduced by 50%

#### Ordering Code: Logic Symbols

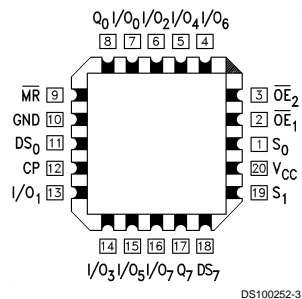


#### Connection Diagrams

Pin Assignment  
for DIP and Flatpak



Pin Assignment for LCC



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FACT® is a registered trademark of Fairchild Semiconductor Corporation.

## Connection Diagrams (Continued)

Pin Names	Description
CP	Clock Pulse Input
DS <sub>0</sub>	Serial Data Input for Right Shift
DS <sub>7</sub>	Serial Data Input for Left Shift
S <sub>0</sub> , S <sub>1</sub>	Mode Select Inputs
$\overline{MR}$	Asynchronous Master Reset
$\overline{OE}_1$ , $\overline{OE}_2$	TRI-STATE Output Enable Inputs
I/O <sub>0</sub> –I/O <sub>7</sub>	Parallel Data Inputs or TRI-STATE Parallel Outputs
Q <sub>0</sub> , Q <sub>7</sub>	Serial Outputs

## Functional Description

The 'AC/ACT299 contains eight edge-triggered D-type flip-flops and the interstage logic necessary to perform synchronous shift left, shift right, parallel load and hold operations. The type of operation is determined by S<sub>0</sub> and S<sub>1</sub>, as shown in the Truth Table. All flip-flop outputs are brought out through TRI-STATE buffers to separate I/O pins that also serve as data inputs in the parallel load mode. Q<sub>0</sub> and Q<sub>7</sub> are also brought out on other pins for expansion in serial shifting of longer words.

A LOW signal on  $\overline{MR}$  overrides the Select and CP inputs and resets the flip-flops. All other state changes are initiated by the rising edge of the clock. Inputs can change when the clock is in either state provided only that the recommended setup and hold times, relative to the rising edge of CP, are observed.

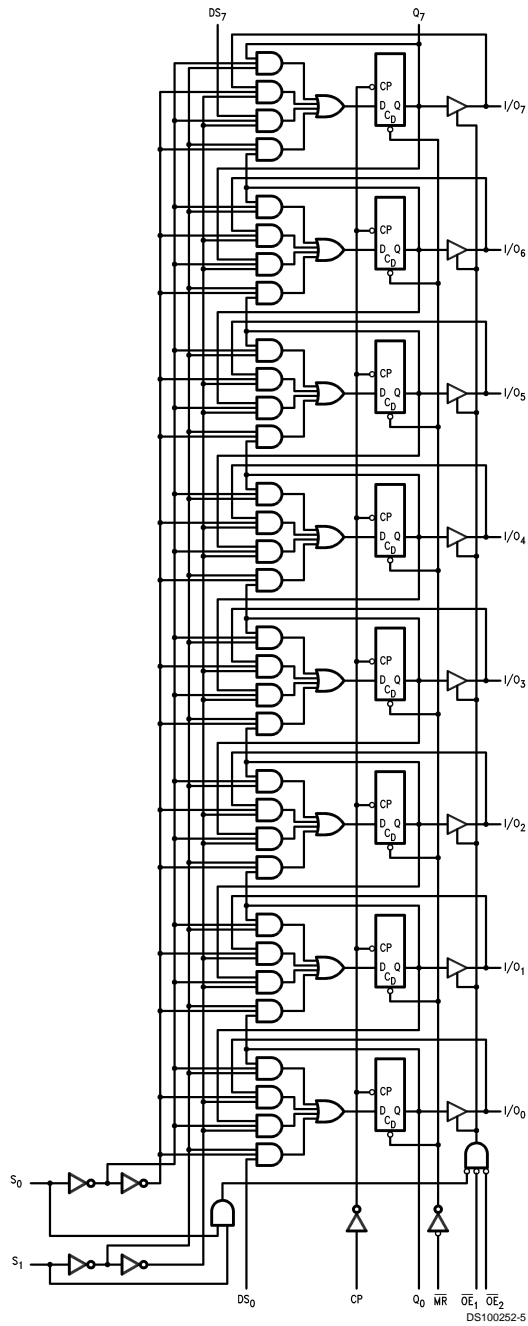
A HIGH signal on either  $\overline{OE}_1$  or  $\overline{OE}_2$  disables the TRI-STATE buffers and puts the I/O pins in the high impedance state. In this condition the shift, hold, load and reset operations can still occur. The TRI-STATE buffers are also disabled by HIGH signals on both S<sub>0</sub> and S<sub>1</sub> in preparation for a parallel load operation.

## Truth Table

Inputs				Response
$\overline{MR}$	S <sub>1</sub>	S <sub>0</sub>	CP	
L	X	X	X	Asynchronous Reset; Q <sub>0</sub> –Q <sub>7</sub> = LOW
H	H	H	↗	Parallel Load; I/O <sub>n</sub> → Q <sub>n</sub>
H	L	H	↗	Shift Right; DS <sub>0</sub> → Q <sub>0</sub> , Q <sub>0</sub> → Q <sub>1</sub> , etc.
H	H	L	↗	Shift Left, DS <sub>7</sub> → Q <sub>7</sub> , Q <sub>7</sub> → Q <sub>6</sub> , etc.
H	L	L	X	Hold

H = HIGH Voltage Level  
 L = LOW Voltage Level  
 X = Immaterial  
 ↗ = LOW-to-HIGH Transition

## Logic Diagram



Please note that this diagram is provided only for the understanding of logic operations and should not be used to estimate propagation delays.

## Absolute Maximum Ratings (Note 1)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Supply Voltage ( $V_{CC}$ )	-0.5V to +7.0V
DC Input Diode Current ( $I_{IK}$ )	
$V_I = -0.5V$	-20 mA
$V_I = V_{CC} + 0.5V$	+20 mA
DC Input Voltage ( $V_I$ )	-0.5V to $V_{CC} + 0.5V$
DC Output Diode Current ( $I_{OK}$ )	
$V_O = -0.5V$	-20 mA
$V_O = V_{CC} + 0.5V$	+20 mA
DC Output Voltage ( $V_O$ )	-0.5V to $V_{CC} + 0.5V$
DC Output Source or Sink Current ( $I_O$ )	±50 mA
DC $V_{CC}$ or Ground Current	
Per Output Pin ( $I_{CC}$ or $I_{GND}$ )	±50 mA
Storage Temperature ( $T_{STG}$ )	-65°C to +150°C
Junction Temperature ( $T_J$ )	
CDIP	175°C

## Recommended Operating Conditions

Supply Voltage ( $V_{CC}$ )	(Unless Otherwise Specified)	
'AC		2.0V to 6.0V
'ACT		4.5V to 5.0V
Input Voltage ( $V_I$ )		0V to $V_{CC}$
Output Voltage ( $V_O$ )		0V to $V_{CC}$
Operating Temperature ( $T_A$ )		
54AC/ACT		-55°C to +125°C
Minimum Input Edge Rate ( $\Delta V/\Delta t$ )		
'AC Devices	$V_{IN}$ from 30% to 70% of $V_{CC}$	
'ACT Devices	$V_{CC}$ @ 3.3V, 4.5V, 5.5V	125 mV/ns
Minimum Input Edge Rate ( $\Delta V/\Delta t$ )		
'ACT Devices	$V_{IN}$ from 0.8V to 2.0V	
'ACT Devices	$V_{CC}$ @ 4.5V, 5.5V	125 mV/ns

**Note 1:** Absolute maximum ratings are those values beyond which damage to the device may occur. Obviously the databook specifications should be met, without exception, to ensure that the system design is reliable over its power supply, temperature, and output/input loading variables. National does not recommend operation of FACT® circuits outside databook specifications.

## DC Electrical Characteristics

For 'AC Family Devices

Symbol	Parameter	$V_{CC}$ (V)	54AC	Units	Conditions
			$T_A =$ -55°C to +125°C Guaranteed Limits		
$V_{IH}$	Minimum High Level Input Voltage	3.0	2.1	V	$V_{OUT} = 0.1V$ or $V_{CC} - 0.1V$
		4.5	3.15		
		5.5	3.85		
$V_{IL}$	Maximum Low Level Input Voltage	3.0	0.9	V	$V_{OUT} = 0.1V$ or $V_{CC} - 0.1V$
		4.5	1.35		
		5.5	1.65		
$V_{OH}$	Minimum High Level Output Voltage	3.0	2.9	V	$I_{OUT} = -50 \mu A$
		4.5	4.4		
		5.5	5.4		
$V_{OL}$	Maximum Low Level Output Voltage	3.0	2.4	V	(Note 2) $V_{IN} = V_{IL}$ or $V_{IH}$ $I_{OH} = -12 mA$ $I_{OH} = -24 mA$ $I_{OH} = -24 mA$
		4.5	3.7		
		5.5	4.7		
$V_{OL}$	Maximum Low Level Output Voltage	3.0	0.1	V	$I_{OUT} = 50 \mu A$
		4.5	0.1		
		5.5	0.1		
$V_{OL}$	Maximum Low Level Output Voltage	3.0	0.50	V	(Note 2) $V_{IN} = V_{IL}$ or $V_{IH}$ $I_{OH} = 12 mA$ $I_{OH} = 24 mA$ $I_{OH} = 24 mA$
		4.5	0.50		
		5.5	0.50		
$I_{IN}$	Maximum Input Leakage Current	5.5	±1.0	µA	$V_I = V_{CC}, GND$

**Note 2:** All outputs loaded; threshold on input associated with output under test.

## DC Electrical Characteristics

For 'AC Family Devices

Symbol	Parameter	V <sub>CC</sub> (V)	54AC	Units	Conditions
			T <sub>A</sub> = -55°C to +125°C		
			Guaranteed Limits		
I <sub>OLD</sub>	(Note 4) Minimum Dynamic	5.5	50	mA	V <sub>OLD</sub> = 1.65V Max
I <sub>OHD</sub>	Output Current	5.5	-50	mA	V <sub>OHD</sub> = 3.85V Min
I <sub>CC</sub>	Maximum Quiescent Supply Current	5.5	80.0	μA	V <sub>IN</sub> = V <sub>CC</sub> or GND
I <sub>OZT</sub>	Maximum I/O Leakage Current	5.5	±5.5	μA	V <sub>I(OE)</sub> = V <sub>IL</sub> , V <sub>IH</sub> V <sub>I</sub> = V <sub>CC</sub> , GND V <sub>O</sub> = V <sub>CC</sub> , GND

**Note 3:** All outputs loaded; threshold on input associated with output under test.

**Note 4:** Maximum test duration 20 ms, one output loaded at a time.

**Note 5:** I<sub>IN</sub> and I<sub>CC</sub> @ 3.0V are guaranteed to be less than or equal to the respective limit @ 5.5V V<sub>CC</sub>.  
I<sub>CC</sub> for 54AC @ 25°C is identical to 74AC @ 25°C.

## DC Electrical Characteristics

For 'ACT Family Devices

Symbol	Parameter	V <sub>CC</sub> (V)	54ACT	Units	Conditions
			T <sub>A</sub> = -55°C to +125°C		
			Guaranteed Limits		
V <sub>IH</sub>	Minimum High Level Input Voltage	4.5	2.0	V	V <sub>OUT</sub> = 0.1V or V <sub>CC</sub> - 0.1V
		5.5	2.0		
V <sub>IL</sub>	Maximum Low Level Input Voltage	3.0	0.8		V <sub>OUT</sub> = 0.1V or V <sub>CC</sub> - 0.1V
		4.5	0.8		
V <sub>OH</sub>	Minimum High Level	4.5	4.4	V	I <sub>OUT</sub> = -50 μA
		5.5	5.4		
		4.5	3.70	V	(Note 7) V <sub>IN</sub> = V <sub>IL</sub> or V <sub>IH</sub> I <sub>OH</sub> = -24 mA I <sub>OH</sub> = -24 mA
		5.5	4.70		
V <sub>OL</sub>	Maximum Low Level Output Voltage	4.5	0.1	V	I <sub>OUT</sub> = 50 μA
		5.5	0.1		
		4.5	0.50	V	(Note 7) V <sub>IN</sub> = V <sub>IL</sub> or V <sub>IH</sub> I <sub>OL</sub> = 24 mA I <sub>OL</sub> = 24 mA
		5.5	0.50		
I <sub>IN</sub>	Maximum Input Leakage Current	5.5	±1.0	μA	V <sub>I</sub> = V <sub>CC</sub> , GND
I <sub>CC</sub> T	Maximum I <sub>CC</sub> /Input	5.5	1.6	mA	V <sub>I</sub> = V <sub>CC</sub> - 2.1V
I <sub>OLD</sub>	(Note 8) Minimum Dynamic	5.5	50	mA	V <sub>OLD</sub> = 1.65V Max
	Output Current				
I <sub>OHD</sub>	Output Current	5.5	-50	mA	V <sub>OHD</sub> = 3.85V Min
I <sub>CC</sub>	Maximum Quiescent Supply Current	5.5	80.0	μA	V <sub>IN</sub> = V <sub>CC</sub> or GND
I <sub>OZT</sub>	Maximum I/O Leakage Current	5.5	±5.0	μA	V <sub>I(OE)</sub> = V <sub>IL</sub> , V <sub>IH</sub> V <sub>I</sub> = V <sub>CC</sub> , GND V <sub>O</sub> = V <sub>CC</sub> , GND

## DC Electrical Characteristics (Continued)

**Note 6:**  $I_{CC}$  limit for 54ACT @ 25°C is identical to 74ACT @ 25°C.

**Note 7:** All outputs loaded; thresholds on input associated with output under test.

**Note 8:** Maximum test duration 2.0 ms, one output loaded at a time.

## Capacitance

Symbol	Parameter	Typ	Units	Conditions
$C_{IN}$	Input Capacitance	4.5	pF	$V_{CC} = 5.0V$
$C_{PD}$	Power Dissipation Capacitance	170	pF	$V_{CC} = 5.5V$

## AC Electrical Characteristics

Symbol	Parameter	$V_{CC}$ (V) (Note 9)	54AC		Units	Fig. No.
			$T_A = -55^\circ C$ to $+125^\circ C$ $C_L = 50$ pF			
			Min	Max		
$f_{max}$	Maximum Input Frequency	3.3	70		MHz	
		5.0	80			
$t_{PLH}$	Propagation Delay CP to $Q_0$ or $Q_7$ (Shift Left or Right)	3.3	1.0	25.5	ns	
		5.0	1.0	17.5		
$t_{PHL}$	Propagation Delay CP to $Q_0$ or $Q_7$ (Shift Left or Right)	3.3	1.0	26.5	ns	
		5.0	1.0	18.0		
$t_{PLH}$	Propagation Delay $\overline{CP}$ to $I/O_n$	3.3	1.0	24.5	ns	
		5.0	1.0	17.0		
$t_{PHL}$	Propagation Delay $\overline{CP}$ to $I/O_n$	3.3	1.0	26.5	ns	
		5.0	1.0	18.5		
$t_{PHL}$	Propagation Delay $\overline{MR}$ to $Q_0$ or $Q_7$	3.3	1.0	27.0	ns	
		5.0	1.0	18.5		
$t_{PHL}$	Propagation Delay $\overline{MR}$ to $I/O_n$	3.3	1.0	26.5	ns	
		5.0	1.0	18.0		
$t_{PZH}$	Output Enable Time $\overline{OE}$ to $I/O_n$	3.3	1.0	22.0	ns	
		5.0	1.0	15.0		
$t_{PZL}$	Output Enable Time $\overline{OE}$ to $I/O_n$	3.3	1.0	23.5	ns	
		5.0	1.0	16.0		
$t_{PHZ}$	Output Disable Time $\overline{OE}$ to $I/O_n$	3.3	1.0	22.5	ns	
		5.0	1.0	17.0		
$t_{PLZ}$	Output Disable Time $\overline{OE}$ to $I/O_n$	3.3	1.0	21.5	ns	
		5.0	1.0	16.0		

**Note 9:** Voltage Range 3.3 is 3.3V  $\pm 0.3V$ .

Voltage Range 5.0 is 5.0V  $\pm 0.5V$ .

## AC Operating Requirements

Symbol	Parameter	V <sub>CC</sub> (V) (Note 10)	54AC		Units	Fig. No.
			T <sub>A</sub> = -55°C to +125°C C <sub>L</sub> = 50 pF			
			Guaranteed Minimum			
t <sub>s</sub>	Setup Time, HIGH or LOW S <sub>0</sub> or S <sub>1</sub> to CP	3.3	9.5		ns	
		5.0	7.0			
t <sub>h</sub>	Hold Time, HIGH or LOW S <sub>0</sub> or S <sub>1</sub> to CP	3.3	2.0		ns	
		5.0	2.5			
t <sub>s</sub>	Setup Time, HIGH or LOW I/O <sub>n</sub> to CP	3.3	6.0		ns	
		5.0	4.0			
t <sub>h</sub>	Hold Time, HIGH or LOW I/O <sub>n</sub> to CP	3.3	1.5		ns	
		5.0	2.0			
t <sub>s</sub>	Setup Time, HIGH or LOW DS <sub>0</sub> or DS <sub>7</sub> to CP	3.3	7.5		ns	
		5.0	5.0			
t <sub>h</sub>	Hold Time, HIGH or LOW DS <sub>0</sub> or DS <sub>7</sub> to CP	3.3	1.5		ns	
		5.0	1.5			
t <sub>w</sub>	CP Pulse Width, LOW	3.3	5.5		ns	
		5.0	5.0			
t <sub>w</sub>	MR Pulse Width, LOW	3.3	5.5		ns	
		5.0	5.0			
t <sub>rec</sub>	Recovery Time MR to CP	3.3	2.5		ns	
		5.0	2.5			

**Note 10:** Voltage Range 3.3 is 3.3V ±0.3V  
Voltage Range 5.0 is 5.0V ±0.5V

## AC Electrical Characteristics

Symbol	Parameter	V <sub>CC</sub> (V) (Note 11)	54ACT		Units	Fig. No.
			T <sub>A</sub> = -55°C to +125°C C <sub>L</sub> = 50 pF			
			Min	Max		
f <sub>max</sub>	Maximum Input Frequency	5.0	70		MHz	
t <sub>PLH</sub>	Propagation Delay CP to Q <sub>0</sub> or Q <sub>7</sub> (Shift Left or Right)	5.0	1.0	15.5	ns	
t <sub>PHL</sub>	Propagation Delay CP to Q <sub>0</sub> or Q <sub>7</sub> (Shift Left or Right)	5.0	1.0	16.0	ns	
t <sub>PLH</sub>	Propagation Delay CP to I/O <sub>n</sub>	5.0	1.0	15.0	ns	
t <sub>PHL</sub>	Propagation Delay CP to I/O <sub>n</sub>	5.0	1.0	18.0	ns	
t <sub>PHL</sub>	Propagation Delay MR to Q <sub>0</sub> or Q <sub>7</sub>	5.0	1.0	18.0	ns	
t <sub>PHL</sub>	Propagation Delay MR to I/O <sub>n</sub>	5.0	1.0	17.5	ns	

### AC Electrical Characteristics (Continued)

Symbol	Parameter	V <sub>CC</sub> (V) (Note 11)	54ACT		Units	Fig. No.
			T <sub>A</sub> = -55°C to +125°C C <sub>L</sub> = 50 pF			
			Min	Max		
t <sub>PZH</sub>	Output Enable Time OE to I/O <sub>n</sub>	5.0	1.0	14.0	ns	
t <sub>PZL</sub>	Output Enable Time OE to I/O <sub>n</sub>	5.0	1.0	14.5	ns	
t <sub>PHZ</sub>	Output Disable Time OE to I/O <sub>n</sub>	5.0	1.0	14.5	ns	
t <sub>PLZ</sub>	Output Disable Time OE to I/O <sub>n</sub>	5.0	1.0	14.0	ns	

Note 11: Voltage Range 5.0 is 5.0V ±0.5V

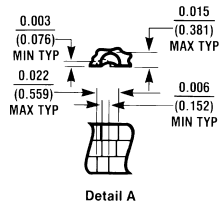
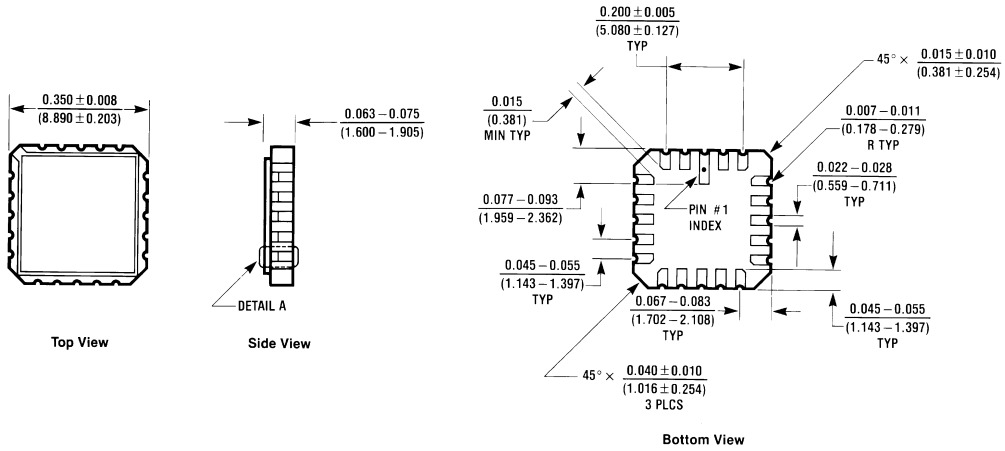
### AC Operating Requirements

Symbol	Parameter	V <sub>CC</sub> (V) (Note 12)	54ACT		Units	Fig. No.
			T <sub>A</sub> = -55°C to +125°C C <sub>L</sub> = 50 pF			
			Guaranteed Minimum			
t <sub>s</sub>	Setup Time, HIGH or LOW S <sub>0</sub> or S <sub>1</sub> to CP	5.0	6.5		ns	
t <sub>h</sub>	Hold Time, HIGH or LOW S <sub>0</sub> or S <sub>1</sub> to CP	5.0	1.5		ns	
t <sub>s</sub>	Setup Time, HIGH or LOW I/O <sub>n</sub> to CP	5.0	4.5		ns	
t <sub>h</sub>	Hold Time, HIGH or LOW I/O <sub>n</sub> to CP	5.0	1.5		ns	
t <sub>s</sub>	Setup Time, HIGH or LOW DS <sub>0</sub> or DS <sub>7</sub> to CP	5.0	5.5		ns	
t <sub>h</sub>	Hold Time, HIGH or LOW DS <sub>0</sub> or DS <sub>7</sub> to CP	5.0	1.5		ns	
t <sub>w</sub>	CP Pulse Width HIGH or LOW	5.0	5.0		ns	
t <sub>w</sub>	MR Pulse Width, LOW	5.0	5.0		ns	
t <sub>rec</sub>	Recovery Time MR to CP	5.0	1.5		ns	

Note 12: Voltage Range 5.0 is 5.0V ±0.5V.

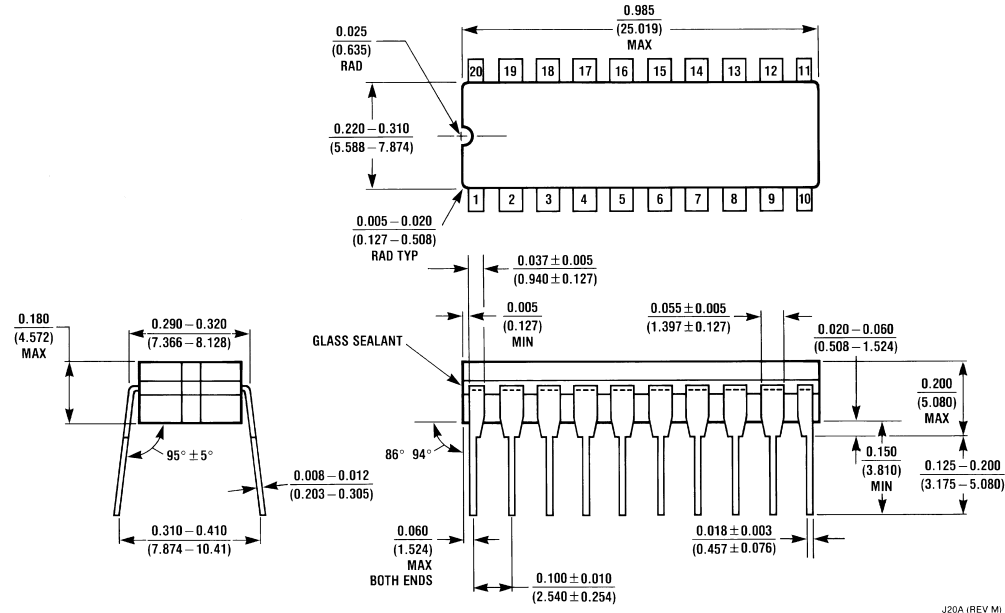


**Physical Dimensions** inches (millimeters) unless otherwise noted



**20 Terminal Ceramic Leadless Chip Carrier (LCC)**  
 NS Package Number E20A

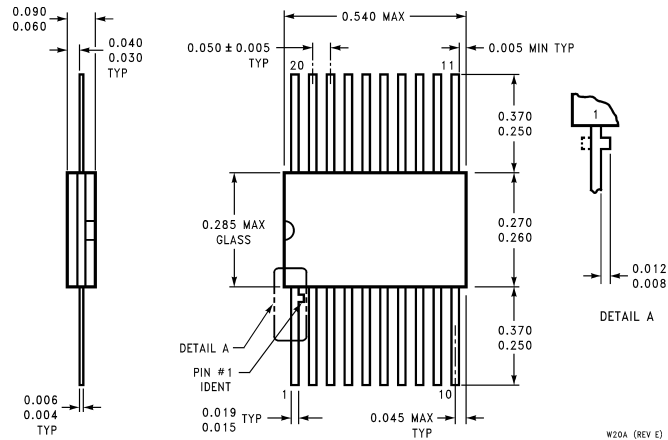
E20A (REV D)



**20 Lead Ceramic Dual-In-Line Package (J)**  
 NS Package Number J20A

J20A (REV M)

**Physical Dimensions** inches (millimeters) unless otherwise noted (Continued)



**20 Lead Ceramic FLATPAK  
NS Package Number W20A**

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