

54F219,74F219

54F219 74F219 64-Bit Random Access Memory with TRI-STATE(RM) Outputs



Literature Number: SNOS173A

54F/74F219 64-Bit Random Access Memory with TRI-STATE® Outputs

General Description

The 'F219 is a high-speed 64-bit RAM organized as a 16-word by 4-bit array. Address inputs are buffered to minimize loading and are fully decoded on-chip. The outputs are TRI-STATE and are in the high-impedance state whenever the Chip Select (\overline{CS}) input is HIGH. The outputs are active only in the Read mode. This device is similar to the 'F189 but features non-inverting, rather than inverting, data outputs.

Features

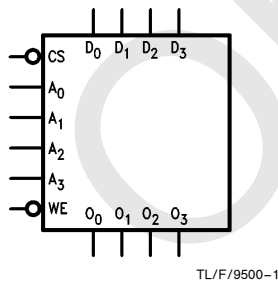
- TRI-STATE outputs for data bus applications
- Buffered inputs minimize loading
- Address decoding on-chip
- Diode clamped inputs minimize ringing
- Available in SOIC (300 mil only)

Commercial	Military	Package Number	Package Description
74F219PC		N16E	16-Lead (0.300" Wide) Molded Dual-In-Line
	54F219DL (Note 2)	J16A	16-Lead Ceramic Dual-In-Line
74F219SC (Note 1)		M16B	16-Lead (0.300" Wide) Molded Small Outline, JEDEC
74F219SJ (Note 1)		M16D	16-Lead (0.300" Wide) Molded Small Outline, EIAJ
	54F219FL (Note 2)	W16A	16-Lead Cerpack
	54F219LL (Note 2)	E20A	20-Lead Ceramic Leadless Chip Carrier, Type C

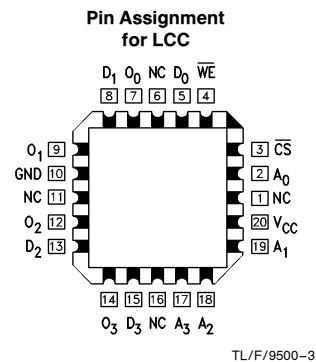
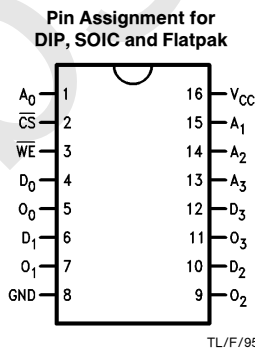
Note 1: Devices also available in 13" reel. Use suffix = SCX and SJX.

Note 2: Military grade device with environmental and burn-in processing. Use suffix = DLQB, FLQB and LLQB.

Logic Symbol



Connection Diagrams



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Unit Loading/Fan Out

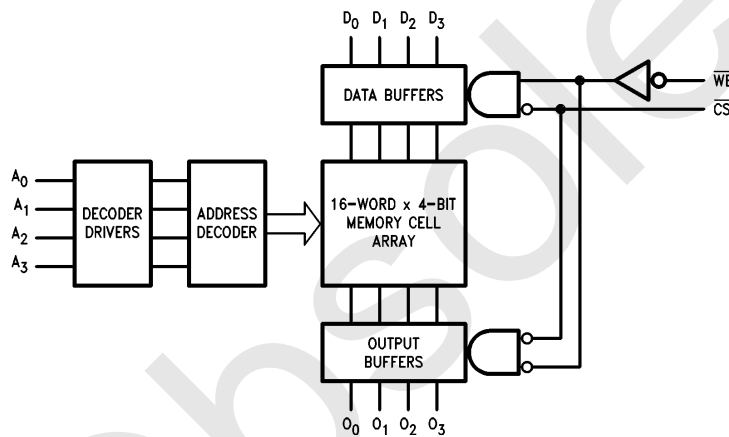
Pin Names	Description	54F/74F	
		U.L. HIGH/LOW	Input I_{IH}/I_{IL} Output I_{OH}/I_{OL}
A_0-A_3	Address Inputs	1.0/1.0	$20 \mu A / -0.6 \text{ mA}$
\overline{CS}	Chip Select Input (Active LOW)	1.0/2.0	$20 \mu A / -1.2 \text{ mA}$
\overline{WE}	Write Enable Input (Active LOW)	1.0/1.0	$20 \mu A / -0.6 \text{ mA}$
D_0-D_3	Data Inputs	1.0/1.0	$20 \mu A / -0.6 \text{ mA}$
O_0-O_3	TRI-STATE Data Outputs	150/40 (33.3)	$-3 \text{ mA} / 24 \text{ mA} (20 \text{ mA})$

Function Table

Inputs		Operation	Condition of Outputs
\overline{CS}	\overline{WE}		
L	L	Write	High Impedance
L	H	Read	True Stored Data
H	X	Inhibit	High Impedance

H = HIGH Voltage Level
L = LOW Voltage Level
X = Immaterial

Block Diagram



TL/F/9500-4

Absolute Maximum Ratings (Note 1)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Storage Temperature	-65°C to +150°C
Ambient Temperature under Bias	-55°C to +125°C
Junction Temperature under Bias	-55°C to +175°C
Plastic	-55°C to +150°C
V _{CC} Pin Potential to Ground Pin	-0.5V to +7.0V
Input Voltage (Note 2)	-0.5V to +7.0V
Input Current (Note 2)	-30 mA to +5.0 mA
Voltage Applied to Output in HIGH State (with V _{CC} = 0V)	
Standard Output	-0.5V to V _{CC}
TRI-STATE Output	-0.5V to +5.5V

Current Applied to Output in LOW State (Max) twice the rated I_{OL} (mA)

Note 1: Absolute maximum ratings are values beyond which the device may be damaged or have its useful life impaired. Functional operation under these conditions is not implied.

Note 2: Either voltage limit or current limit is sufficient to protect inputs.

Recommended Operating Conditions

Free Air Ambient Temperature	
Military	-55°C to +100°C
Commercial	0°C to +70°C
Supply Voltage	
Military	+4.5V to +5.5V
Commercial	+4.5V to +5.5V

DC Electrical Characteristics

Symbol	Parameter		54F/74F			Units	V _{CC}	Conditions
			Min	Typ	Max			
V _{IH}	Input HIGH Voltage		2.0			V		Recognized as a HIGH Signal
V _{IL}	Input LOW Voltage		0.8			V		Recognized as a LOW Signal
V _{CD}	Input Clamp Diode Voltage		-1.2			V	Min	I _{IN} = -18 mA
V _{OH}	Output HIGH Voltage	54F 10% V _{CC}	2.5			V	Min	I _{OH} = -1 mA I _{OH} = -3 mA I _{OH} = -1 mA I _{OH} = -3 mA I _{OH} = -1 mA I _{OH} = -3 mA
		54F 10% V _{CC}	2.4					
		74F 10% V _{CC}	2.5					
		74F 10% V _{CC}	2.4					
		74F 5% V _{CC}	2.7					
		74F 5% V _{CC}	2.7					
V _{OL}	Output LOW Voltage	54F 10% V _{CC}	0.5			V	Min	I _{OL} = 20 mA I _{OL} = 24 mA
		74F 10% V _{CC}	0.5					
I _{IH}	Input HIGH Current	54F	20.0			μA	Max	V _{IN} = 2.7V
		74F	5.0					
I _{BVI}	Input HIGH Current Breakdown Test	54F	100			μA	Max	V _{IN} = 7.0V
		74F	7.0					
I _{CEX}	Output HIGH Leakage Current	54F	250			μA	Max	V _{OUT} = V _{CC}
		74F	50					
V _{ID}	Input Leakage Test	74F	4.75			V	0.0	I _{ID} = 1.9 μA All Other Pins Grounded
I _{OD}	Output Leakage Circuit Current	74F	3.75			μA	0.0	V _{IOD} = 150 mV All Other Pins Grounded
I _{IL}	Input LOW Current		-0.6 -1.2			mA	Max	V _{IN} = 0.5V (A _n , \overline{WE} , D _n) V _{IN} = 0.5V (CS)
I _{OZH}	Output Leakage Current		50			μA	Max	V _{OUT} = 2.7V
I _{OZL}	Output Leakage Current		-50			μA	Max	V _{OUT} = 0.5V
I _{OS}	Output Short-Circuit Current		-60 -150			mA	Max	V _{OUT} = 0V
I _{ZZ}	Bus Drainage Test		500			μA	0.0V	V _{OUT} = 5.25V
I _{CC}	Power Supply Current		37 55			mA	Max	

AC Electrical Characteristics

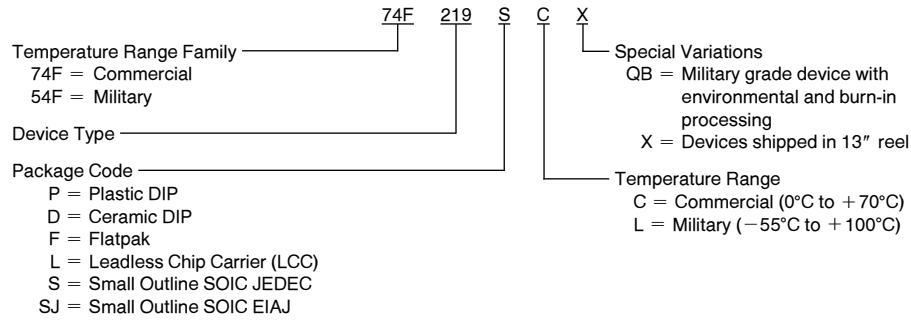
Symbol	Parameter	74F			54F		74F		Units
		$T_A = +25^\circ\text{C}$ $V_{CC} = +5.0\text{V}$ $C_L = 50\text{ pF}$			$T_A = +100^\circ\text{C}$ $V_{CC} = \text{Mil}$ $C_L = 50\text{ pF}$		$T_A, V_{CC} = \text{Com}$ $C_L = 50\text{ pF}$		
		Min	Typ	Max	Min	Max	Min	Max	
t_{PLH} t_{PHL}	Access Time, HIGH or LOW A_n to O_n	10.0 8.0	18.5 13.5	26.0 19.0	9.0 8.0	32.0 23.0	10.0 8.0	27.0 20.0	ns
t_{PZH} t_{PZL}	Access Time, HIGH or LOW \overline{CS} to O_n	3.5 5.0	6.0 9.0	8.5 13.0	3.5 5.0	10.5 15.0	3.5 5.0	9.5 14.0	ns
t_{PHZ} t_{PLZ}	Disable Time, HIGH or LOW \overline{CS} to O_n	2.0 3.0	4.0 5.5	6.0 8.0	2.0 2.5	8.0 10.0	2.0 3.0	7.0 9.0	ns
t_{PZH} t_{PZL}	Write Recovery Time HIGH or LOW, \overline{WE} to O_n	6.5 6.5	20.0 11.0	28.0 15.5	6.5 6.5	37.5 17.5	6.5 6.5	29.0 16.5	ns
t_{PHZ} t_{PLZ}	Disable Time, HIGH or LOW \overline{WE} to O_n	4.0 5.0	7.0 9.0	10.0 13.0	3.5 5.0	12.0 15.0	4.0 5.0	11.0 14.0	ns

AC Operating Requirements

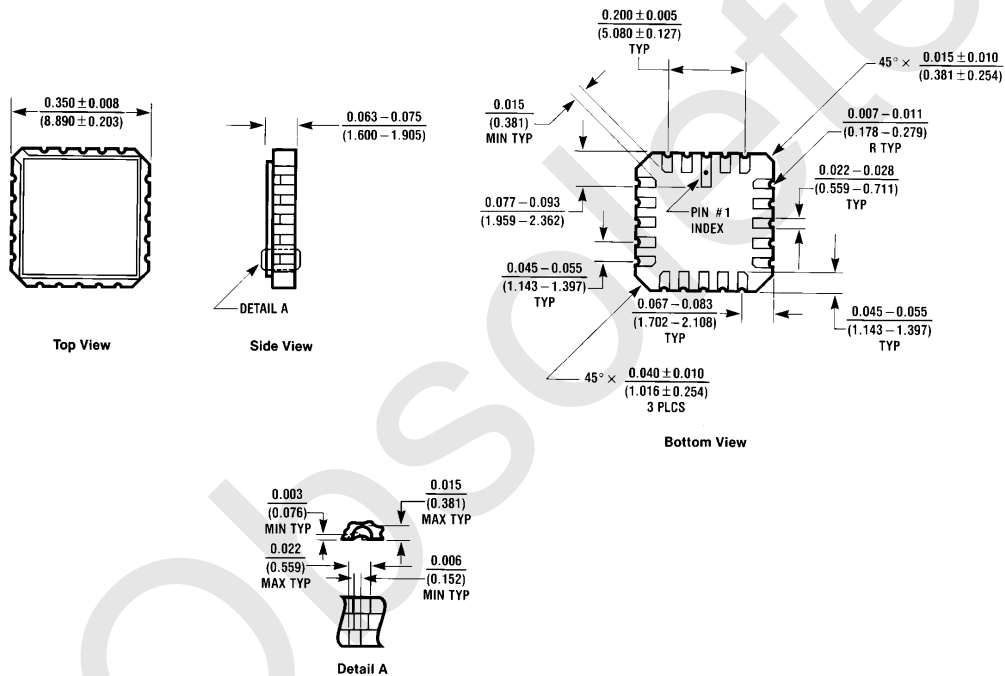
Symbol	Parameter	74F		54F		74F		Units
		$T_A = +25^\circ\text{C}$ $V_{CC} = +5.0\text{V}$		$T_A = +100^\circ\text{C}$ $V_{CC} = \text{Mil}$		$T_A, V_{CC} = \text{Com}$		
		Min	Max	Min	Max	Min	Max	
$t_s(H)$ $t_s(L)$	Setup Time, HIGH or LOW A_n to \overline{WE}	0 0		0 0		0 0		ns
$t_h(H)$ $t_h(L)$	Hold Time, HIGH or LOW A_n to \overline{WE}	2.0 2.0		2.0 2.0		2.0 2.0		ns
$t_s(H)$ $t_s(L)$	Setup Time, HIGH or LOW D_n to \overline{WE}	10.0 10.0		11.0 11.0		10.0 10.0		ns
$t_h(H)$ $t_h(L)$	Hold Time, HIGH or LOW D_n to \overline{WE}	0 0		2.0 2.0		0 0		ns
$t_s(L)$	Setup Time, LOW \overline{CS} to \overline{WE}	0		0		0		ns
$t_h(L)$	Hold Time, LOW \overline{CS} to \overline{WE}	6.0		7.5		6.0		ns
$t_w(L)$	\overline{WE} Pulse Width, LOW	6.0		15.0		6.0		ns

Ordering Information

The device number is used to form part of a simplified purchasing code where the package type and temperature range are defined as follows:



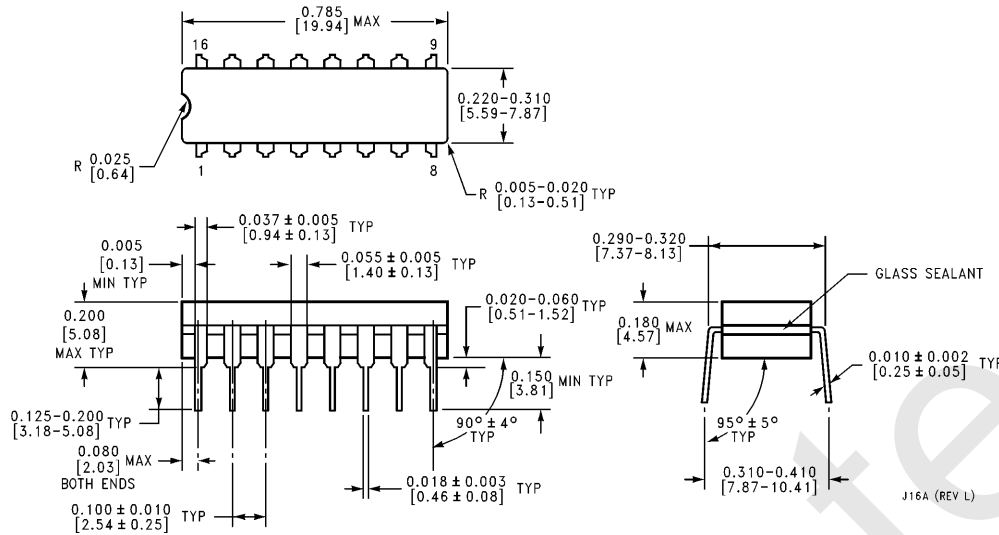
Physical Dimensions inches (millimeters)



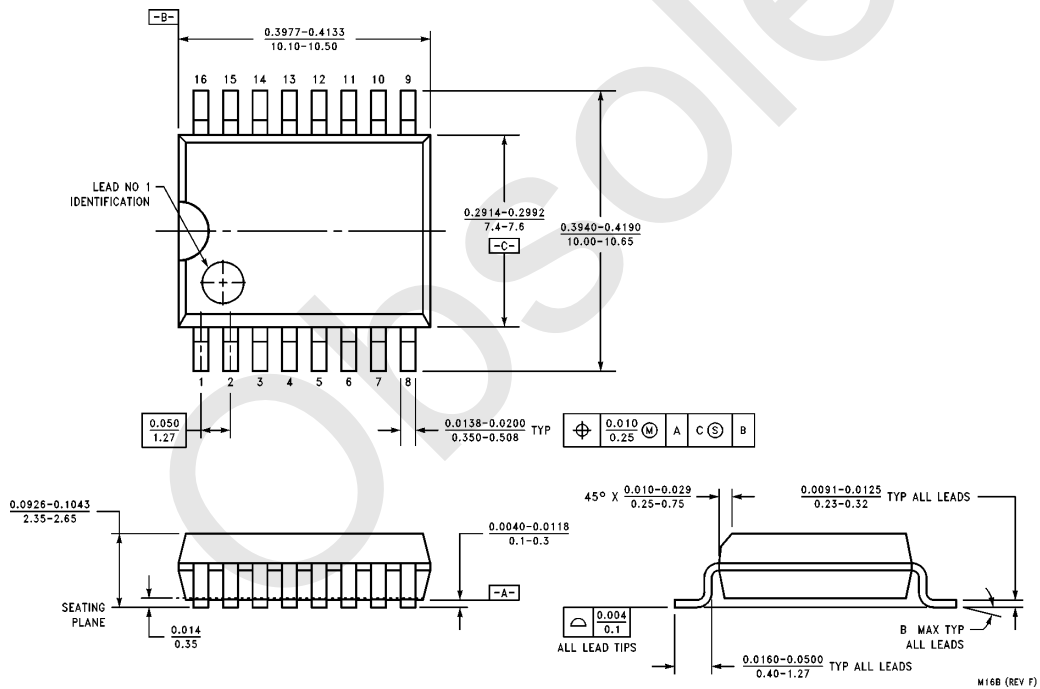
20-Lead Ceramic Leadless Chip Carrier (L)
NS Package Number E20A

E20A (REV D)

Physical Dimensions inches (millimeters) (Continued)

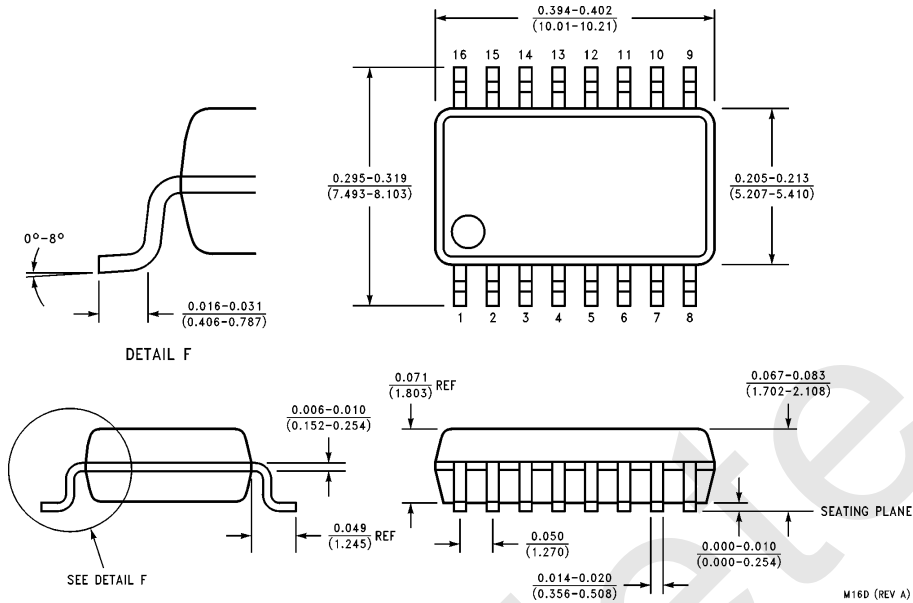


**16-Lead Ceramic Dual-In-Line Package (D)
NS Package Number J16A**

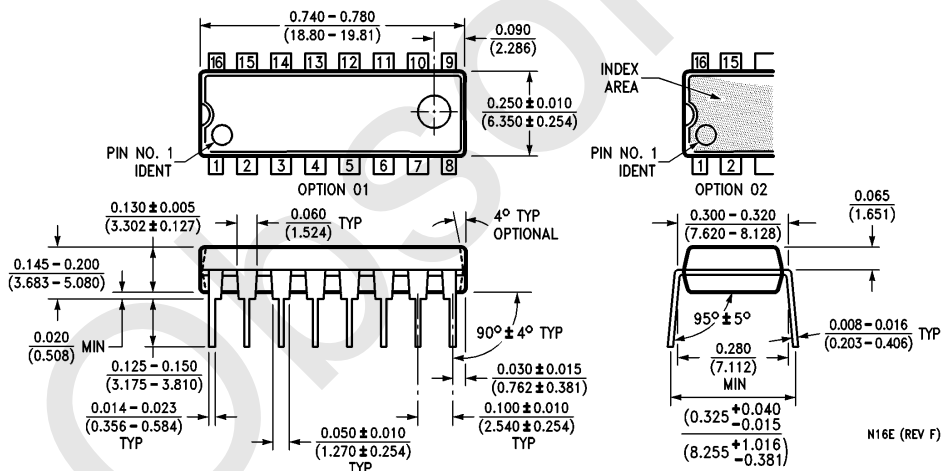


**16-Lead (0.300" Wide) Molded Small Outline Package, JEDEC (S)
NS Package Number M16B**

Physical Dimensions inches (millimeters) (Continued)

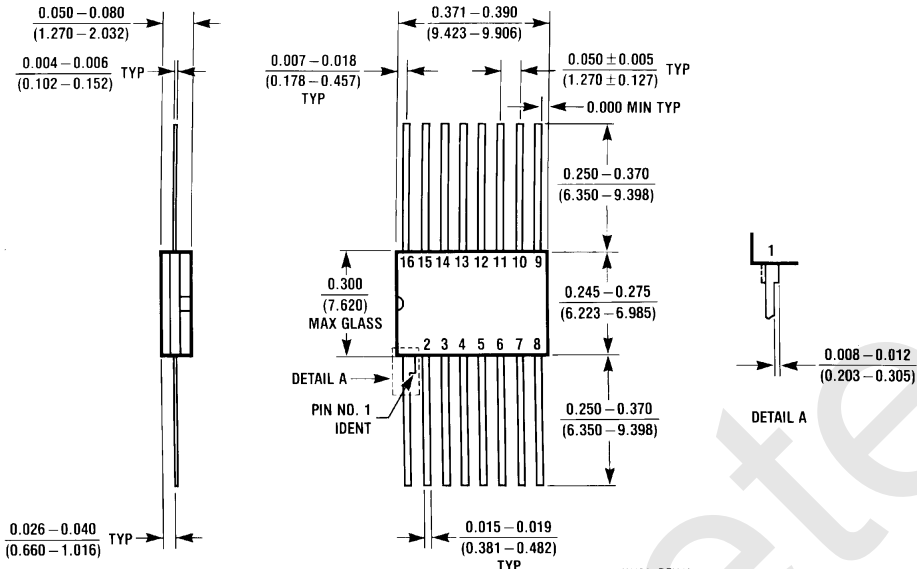


**16-Lead (0.300" Wide) Molded Small Outline Package, EIAJ (SJ)
NS Package Number M16D**



**16-Lead (0.300" Wide) Molded Dual-In-Line Package (P)
NS Package Number N16E**

Physical Dimensions inches (millimeters) (Continued)



16-Lead Ceramic Flatpak (F)
NS Package Number W16A

W16A (REV. H)

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