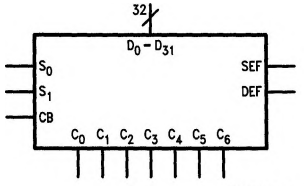
National Semiconductor

54F/74F420
Parallel Check Bit/Syndrome Bit Generator

General Description

The 'F420 is a parallel check bit/syndrome bit generator. The 'F420 utilizes a modified hamming code to generate 7 check bits from a 32-bit dataword, in 15 ns, when operated in the check bit generate mode. When operated in the syndrome generate mode, the check bits and data bits read from memory are utilized in a parity summer to generate syndrome bits upon error detection. The maximum error count detectable is 2. A single error detect can occur in 18 ns; a double error detect in 22 ns. The syndrome bit generation can be output in 15 ns (maximum).

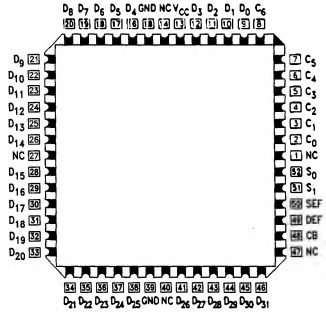
Logic Diagram



TL/F/9542–1

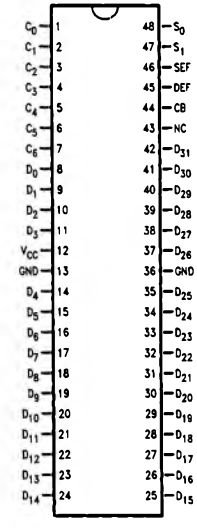
Connection Diagrams

Pin Assignment for LCC and PCC



TL/F/9542–2

Pin Assignment for DIP and Flatpak



TL/F/9542–3

Unit Loading/Fan Out: See Section 1 for U.L. definitions

Pin Names	Description	54F/74F	
		U.L. HIGH/LOW	Input I_{IH}/I_{IL} Output I_{OH}/I_{OL}
C_0–C_6	Check Bit/Syndrome Bus Inputs/ Outputs	3.5/1.083 150/40 (33.3)	70 μA/−0.65 mA −3 mA/24 mA (20 mA)
D_0–D_{31}	Data Bit Bus	1.0/1.0	20 μA/−0.6 mA
CB	Check Bit Control	1.0/1.0	20 μA/−0.6 mA
DEF	Double Error Flag	50/33.3	−1 mA/20 mA
SEF	Single Error Flag	50/33.3	−1 mA/20 mA
S_0, S_1	Mode Control	1.0/1.0	20 μA/−0.6 mA