National Semiconductor

ADVANCE INFORMATION

54FCT/74FCT843A • 54FCT/74FCT843B
9-Bit Transparent Latch

General Description

The 'FCT843A/B bus interface latch is designed to eliminate the extra packages required to buffer existing latches and provide extra data width for wider address/data paths.

FACT™ FCTA/B utilizes NSC quiet series technology to provide improved quiet output switching and dynamic threshold performance.

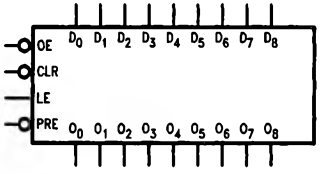
FACT FCTA features GTO™ output control and undershoot corrector in addition to a split ground bus for superior performance.

FACT FCTB features an undershoot corrector in addition to a split ground bus for superior performance.

Features

- NSC 54FCT/74FCT843A/B is pin and functionally equivalent to IDT 54FCT/74FCT843A/B
- High Speed parallel latches
- Buffered common latch enable, clear and preset inputs
- Input clamp diodes to limit bus reflections
- TTL/CMOS input and output level compatible
- I_{OL} = 48 mA (Com), 32 mA (Mil)
- CMOS power levels
- 4 kV minimum ESD immunity
- Military Product compliant to MIL-STD 883

Logic Symbols



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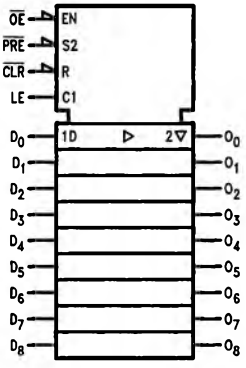
Pin Names	Description
D_0–D_7	Data Inputs
O_0–O_7	Data Outputs
$\overline{OE}$	Output Enable
LE	Latch Enable
$\overline{CLR}$	Clear
$\overline{PRE}$	Preset



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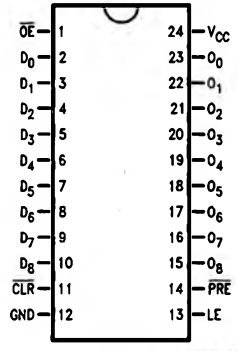
Connection Diagrams

Pin Assignment for DIP, Flatpak and SOIC



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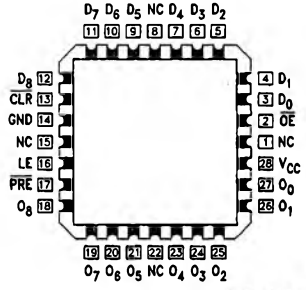
Pin Assignment for LCC



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