54H/74H106

DUAL JK EDGE-TRIGGERED FLIP-FLOP

(With Separate Sets, Clear and Clocks)

DESCRIPTION — The '106 is a high speed JK negative edge-triggered flip-flop. It features individual J, K, clock and asynchronous set and clear inputs to each flip-flop. When the clock goes HIGH, the inputs are enabled and data will be accepted. The logic state of J and K inputs may be allowed to change when the clock pulse is in a HIGH state and the bistable will perform according to the Truth Table as long as minimum setup times are observed. Input data is transferred to the outputs on the falling edge of the clock pulse.

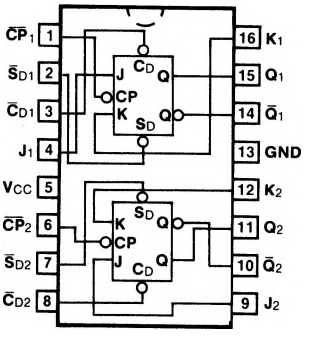
TRUTH TABLE

INPUTS		OUTPUT
@ t_n		@ t_{n+1}
J	K	Q
L	L	Q_n
L	H	L
H	L	H
H	H	$\overline{Q}_n$

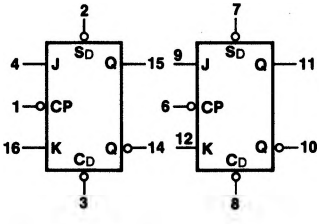
Asynchronous Inputs:
LOW input to $\overline{S}_D$ sets Q to HIGH level
LOW input to $\overline{C}_D$ sets Q to LOW level
Clear and Set are independent of clock
Simultaneous LOW on $\overline{C}_D$ and $\overline{S}_D$ makes both Q and $\overline{Q}$ HIGH

t_n = Bit time before clock pulse.
t_{n+1} = Bit time after clock pulse.
H = HIGH Voltage Level
L = LOW Voltage Level

CONNECTION DIAGRAM
PINOUT A



LOGIC SYMBOL



V_{CC} = Pin 5
GND = Pin 13

ORDERING CODE: See Section 9

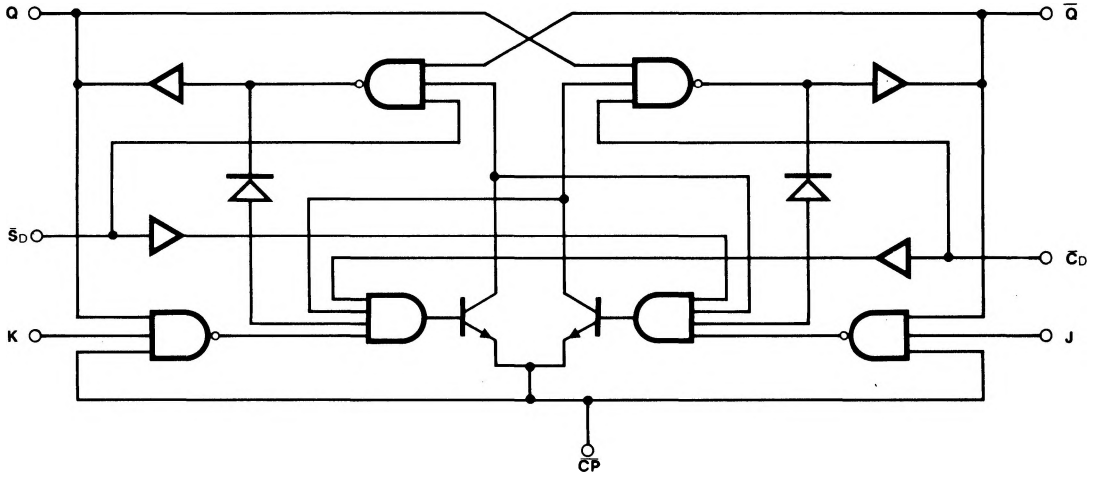
PKGS	PIN OUT	COMMERCIAL GRADE: V_{CC} = +5.0 V ±5%, T_A = 0°C to +70°C	MILITARY GRADE: V_{CC} = +5.0 V ±10%, T_A = -55°C to +125°C	PKG TYPE
Plastic DIP (P)	A	74H106PC		9B
Ceramic DIP (D)	A	74H106DC	54H106DM	6B
Flatpak (F)	A	74H106FC	54H106FM	4L

INPUT LOADING/FAN-OUT: See Section 3 for U.L. definitions

PIN NAMES	DESCRIPTION	54/74H (U.L.) HIGH/LOW
J_1, J_2, K_1, K_2	Data Inputs	1.25/1.25
$\overline{CP}_1$, $\overline{CP}_2$	Clock Pulse Inputs (Active Falling Edge)	0*/3.0
$\overline{C}_{D1}$, $\overline{C}_{D2}$	Direct Clear Inputs (Active LOW)	2.5/1.25
$\overline{S}_{D1}$, $\overline{S}_{D2}$	Direct Set Inputs (Active LOW)	2.5/1.25
Q_1, Q_2, $\overline{Q}_1$, $\overline{Q}_2$	Outputs	12.5/12.5

*$\overline{CP}$ Sourcing Current, see DC Characteristics Table

LOGIC DIAGRAM (one half shown)



DC CHARACTERISTICS OVER OPERATING TEMPERATURE RANGE (unless otherwise specified)

SYMBOL	PARAMETER	54/74H Min	54/74H Max	UNITS	CONDITIONS
I_{IH}	Input HIGH Current at $\overline{CP}_n$	0	-1.0	mA	V_{CC} = Max, V_{CP} = 2.4 V
I_{CC}	Power Supply Current		76	mA	V_{CC} = Max, V_{CP} = 0 V

AC CHARACTERISTICS: V_{CC} = +5.0 V, T_A = +25°C (See Section 3 for waveforms and load configurations)

SYMBOL	PARAMETER	54/74H C_L = 25 pF, R_L = 280 Ω Min	54/74H C_L = 25 pF, R_L = 280 Ω Max	UNITS	CONDITIONS
f_{max}	Maximum Clock Frequency	40		MHz	Figs. 3-1, 3-9
t_{PLH} t_{PHL}	Propagation Delay $\overline{CP}_n$ to Q_n or $\overline{Q}_n$		15 20	ns	Figs. 3-1, 3-9
t_{PLH} t_{PHL}	Propagation Delay $\overline{C}_{Dn}$ or $\overline{S}_{Dn}$ to Q_n or $\overline{Q}_n$		12 20	ns	$V_{CP} \geq$ 2.0 V Figs. 3-1, 3-10
t_{PLH} t_{PHL}	Propagation Delay $\overline{C}_{Dn}$ or $\overline{S}_{Dn}$ to Q_n or $\overline{Q}_n$		12 35	ns	$V_{CP} \leq$ 0.8 V Figs. 3-1, 3-10

AC OPERATING REQUIREMENTS: V_{CC} = +5.0 V, T_A = +25°C

SYMBOL	PARAMETER	54/74H Min	54/74H Max	UNITS	CONDITIONS
t_s (H) t_s (L)	Setup Time J_n or K_n to $\overline{CP}_n$	10 13		ns	Fig. 3-7
t_h (H) t_h (L)	Hold Time J_n or K_n to $\overline{CP}_n$	0 0		ns	
t_w (H) t_w (L)	$\overline{CP}_n$ Pulse Width	10 15		ns	Fig. 3-9
t_w (L)	$\overline{C}_{Dn}$ or $\overline{S}_{Dn}$ Pulse Width LOW	16		ns	Fig. 3-10