

# 54/7472 54H/74H72

## JK MASTER/SLAVE FLIP-FLOP (With AND Inputs)

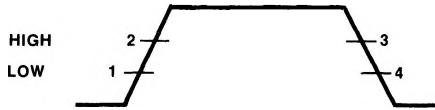
**DESCRIPTION** — The '72 is a high speed JK master/slave flip-flop with AND gate inputs. The AND gate inputs for entry into the master section are controlled by the clock pulse. The clock pulse also regulates the circuitry which connects the master and slave sections. The sequence of operation is as follows: 1) isolate slave from master; 2) enter information from AND gate inputs to master; 3) disable AND gate inputs; 4) transfer information from master to slave. The logic state of J and K inputs must not be allowed to change when the clock pulse is in a HIGH state.

**TRUTH TABLE**

INPUTS		OUTPUT
J	K	Q
L	L	Q <sub>n</sub>
L	H	L
H	L	H
H	H	Q <sub>n</sub>

$J = (J_{1A} \cdot J_{1B}) + (J_{2A} \cdot J_{2B})$   
 $K = (K_{1A} \cdot K_{1B}) + (K_{2A} \cdot K_{2B})$   
 $t_n$  = Bit time before clock pulse.  
 $t_{n+1}$  = Bit time after clock pulse.  
 H = HIGH Voltage level  
 L = LOW Voltage Level

**CLOCK WAVEFORM**



**Asynchronous Inputs:**

LOW input to  $\bar{S}_D$  sets Q to HIGH level  
 LOW input to  $\bar{C}_D$  sets Q to LOW level  
 Clear and Set are independent of clock  
 Simultaneous LOW on  $\bar{C}_D$  and  $\bar{S}_D$  is indeterminate

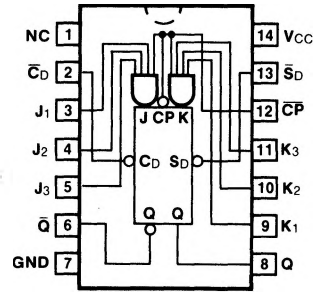
**ORDERING CODE:** See Section 9

PKGS	PIN OUT	COMMERCIAL GRADE	MILITARY GRADE	PKG TYPE
		V <sub>CC</sub> = +5.0 V ±5%, T <sub>A</sub> = 0°C to +70°C	V <sub>CC</sub> = +5.0 V ±10%, T <sub>A</sub> = -55°C to +125°C	
Plastic DIP (P)	A	7472PC, 74H72PC		9A
Ceramic DIP (D)	A	7472DC, 74H72DC	5472DM, 54H72DM	6A
Flatpak (F)	B	7472FC, 74H72FC	5472FM, 54H72FM	3I

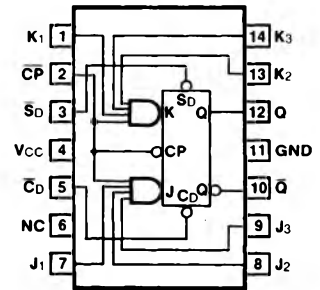
**INPUT LOADING/FAN-OUT:** See Section 3 for U.L. definitions

PIN NAMES	DESCRIPTION	54/74 (U.L.) HIGH/LOW	54/74H (U.L.) HIGH/LOW
J <sub>1</sub> — J <sub>3</sub> , K <sub>1</sub> — K <sub>3</sub>	Data Inputs	1.0/1.0	1.25/1.25
$\bar{C}_P$	Clock Pulse Input (Active Falling Edge)	2.0/2.0	2.5/2.5
$\bar{C}_D$	Direct Clear Input (Active LOW)	2.0/2.0	2.5/2.5
$\bar{S}_D$	Direct Set Input (Active LOW)	2.0/2.0	2.5/2.5
Q, $\bar{Q}$	Outputs	20/10	12.5/12.5

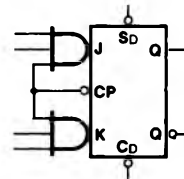
**CONNECTION DIAGRAMS  
PINOUT A**



**PINOUT B**

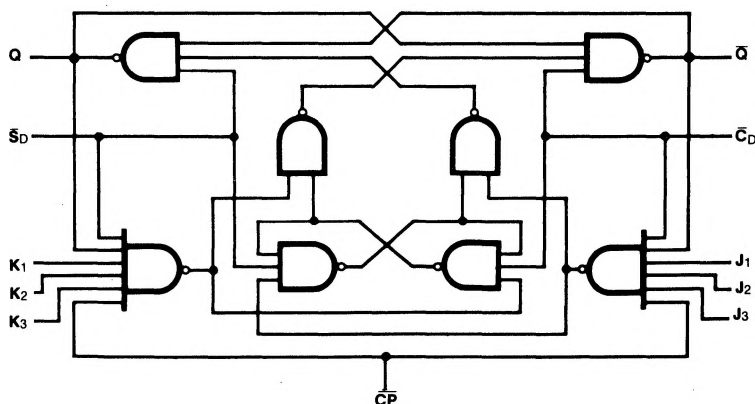


**LOGIC SYMBOL**



V<sub>CC</sub> = Pin 14 (4)  
 GND = Pin 7 (11)  
 NC = Pin 1 (6)

## LOGIC DIAGRAM



## DC CHARACTERISTICS OVER OPERATING TEMPERATURE RANGE (unless otherwise specified)

SYMBOL	PARAMETER	54/74		54/74H		UNITS	CONDITIONS
		Min	Max	Min	Max		
I <sub>CC</sub>	Power Supply Current	20		25		mA	V <sub>CC</sub> = Max, V <sub>CP</sub> = 0 V

AC CHARACTERISTICS: V<sub>CC</sub> = +5.0 V, T<sub>A</sub> = +25°C (See Section 3 for waveforms and load configurations)

SYMBOL	PARAMETER	54/74		54/74H		UNITS	CONDITIONS
		C <sub>L</sub> = 15 pF R <sub>L</sub> = 400 Ω		C <sub>L</sub> = 25 pF R <sub>L</sub> = 280 Ω			
		Min	Max	Min	Max		
f <sub>max</sub>	Maximum Clock Frequency	15		25		MHz	Figs. 3-1, 3-9
t <sub>PLH</sub> t <sub>PHL</sub>	Propagation Delay CP to Q or Q̄	25 40		21 27		ns	Figs. 3-1, 3-9
t <sub>PLH</sub> t <sub>PHL</sub>	Propagation Delay S <sub>D</sub> or C <sub>D</sub> to Q or Q̄	25 40		13 24		ns	Figs. 3-1, 3-10

AC OPERATING REQUIREMENTS: V<sub>CC</sub> = +5.0 V, T<sub>A</sub> = +25°C

SYMBOL	PARAMETER	54/74		54/74H		UNITS	CONDITIONS
		Min	Max	Min	Max		
t <sub>s</sub> (H) t <sub>s</sub> (L)	Setup Time J <sub>n</sub> or K <sub>n</sub> to CP̄	0		0		ns	Fig. 3-18
t <sub>h</sub> (H) t <sub>h</sub> (L)	Hold Time J <sub>n</sub> or K <sub>n</sub> to CP̄	0		0		ns	Fig. 3-18
t <sub>w</sub> (H) t <sub>w</sub> (L)	CP̄ Pulse Width	20 47		12 28		ns	Fig. 3-9
t <sub>w</sub> (L)	S <sub>D</sub> or C <sub>D</sub> Pulse Width LOW	25		16		ns	Fig. 3-10