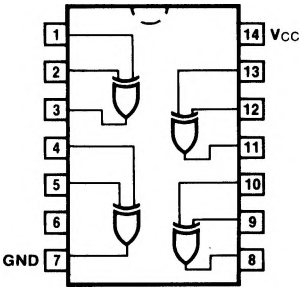
54LS/74LS136

QUAD 2-INPUT EXCLUSIVE-OR GATE

(With Open-Collector Outputs)

CONNECTION DIAGRAM
PINOUT A



ORDERING CODE: See Section 9

PKGS	PIN OUT	COMMERCIAL GRADE V_{CC} = +5.0 V ±5%, T_A = 0°C to +70°C	MILITARY GRADE V_{CC} = +5.0 V ±10%, T_A = -55°C to +125°C	PKG TYPE
Plastic DIP (P)	A	74LS136PC		9A
Ceramic DIP (D)	A	74LS136DC	54LS136DM	6A
Flatpak (F)	A	74LS136FC	54LS136FM	3I

TRUTH TABLE

INPUTS		OUTPUT
A	B	Z
L	L	L
L	H	H
H	L	H
H	H	L

H = HIGH Voltage Level
L = LOW Voltage Level

INPUT LOADING/FAN-OUT: See Section 3 for U.L. definitions

PINS	54/74LS (U.L.) HIGH/LOW
Inputs	1.0/0.375
Outputs	OC**/5.0 (2.5)

DC AND AC CHARACTERISTICS: See Section 3*

SYMBOL	PARAMETER	54/74LS Min	54/74LS Max	UNITS	CONDITIONS
I_{CC}	Power Supply Current		10	mA	V_{CC} = Max
t_{PLH} t_{PHL}	Propagation Delay		23 23	ns	Other Input LOW Figs. 3-2, 3-5
t_{PLH} t_{PHL}	Propagation Delay		23 23	ns	Other Input HIGH Figs. 3-2, 3-4

*DC limits apply over operating temperature range; AC limits apply at T_A = +25°C and V_{CC} = +5.0 V.
**OC — Open Collector