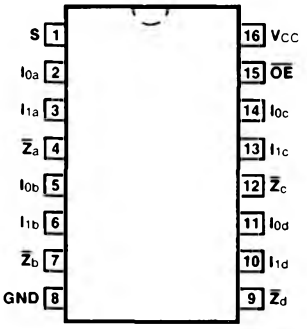
54S/74S258
54LS/74LS258

QUAD 2-INPUT MULTIPLEXER

(With 3-State Outputs)

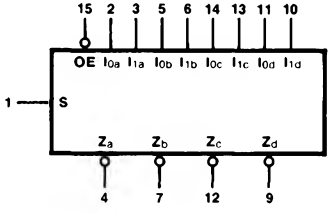
CONNECTION DIAGRAM
PINOUT A



DESCRIPTION — The '258 is a quad 2-input multiplexer with 3-state outputs. Four bits of data from two sources can be selected using a common data select input. The four outputs present the selected data in the complement (inverted) form. The outputs may be switched to a high impedance state with a HIGH on the common Output Enable ($\overline{OE}$) Input, allowing the outputs to interface directly with bus oriented systems. It is fabricated with the Schottky barrier diode process for high speed.

- **SCHOTTKY PROCESS FOR HIGH SPEED**
- **MULTIPLEXER EXPANSION BY TYING OUTPUTS TOGETHER**
- **INVERTING 3-STATE OUTPUTS**

LOGIC SYMBOL



VCC = Pin 16
GND = Pin 8

ORDERING CODE: See Section 9

PKGS	PIN OUT	COMMERCIAL GRADE: VCC = +5.0 V ±5%, TA = 0°C to +70°C	MILITARY GRADE: VCC = +5.0 V ±10%, TA = -55°C to +125°C	PKG TYPE
Plastic DIP (P)	A	74S258PC, 74LS258PC		9B
Ceramic DIP (D)	A	74S258DC, 74LS258DC	54S258DM, 54LS258DM	6B
Flatpak (F)	A	74S258FC, 74LS258FC	54S258FM, 54LS258FM	4L

INPUT LOADING/FAN-OUT: See Section 3 for U.L. defintions

PIN NAMES	DESCRIPTION	54/74S (U.L.) HIGH/LOW	54/74LS (U.L.) HIGH/LOW
$\overline{S}$	Common Data Select Input	2.5/2.5	1.0/0.5
$\overline{OE}$	3-State Output Enable Input (Active LOW)	1.25/1.25	0.5/0.25
$I_{0a} - I_{0d}$	Data Inputs from Source 0	1.25/1.25	0.5/0.25
$I_{1a} - I_{1d}$	Data Inputs from Source 1	1.25/1.25	0.5/0.25
$\overline{Z}_a - \overline{Z}_d$	Inverting Data Outputs	162/12.5 (50)	65/15 (25)/(7.5)

FUNCTIONAL DESCRIPTION — This device is a quad 2-input multiplexer with 3-state outputs. It selects four bits of data from two sources under control of a common Select input (S). When the Select input is LOW, the I_{0x} inputs are selected and when Select is HIGH, the I_{1x} inputs are selected. The data on the selected inputs appears at the outputs in inverted form. The '258 is the logic implementation of a 4-pole, 2-position switch where the position of the switch is determined by the logic levels supplied to the Select input. The logic equations for the outputs are shown below:

$$\overline{Z}_a = \overline{\overline{OE}} \bullet (I_{1a} \bullet S + I_{0a} \bullet \overline{S}) \qquad \overline{Z}_b = \overline{\overline{OE}} \bullet (I_{1b} \bullet S + I_{0b} \bullet \overline{S})$$
$$\overline{Z}_c = \overline{\overline{OE}} \bullet (I_{1c} \bullet S + I_{0c} \bullet \overline{S}) \qquad \overline{Z}_d = \overline{\overline{OE}} \bullet (I_{1d} \bullet S + I_{0d} \bullet \overline{S})$$

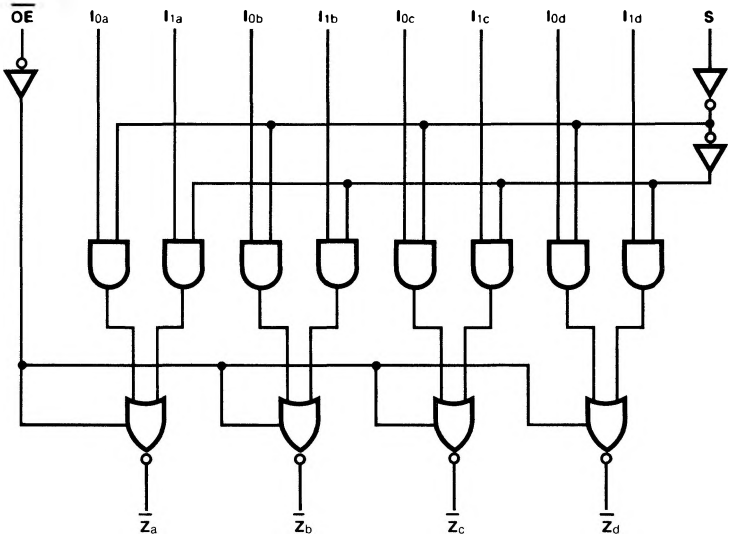
When the Output Enable input ($\overline{OE}$) is HIGH, the outputs are forced to a high impedance OFF state. If the outputs of the 3-state devices are tied together, all but one device must be in the high impedance state to avoid high currents that would exceed the maximum ratings. Designers should ensure that Output Enable signals to 3-state devices whose outputs are tied together are designed so there is no overlap.

TRUTH TABLE

OUTPUT ENABLE	SELECT INPUT	DATA INPUTS		OUTPUTS
$\overline{OE}$	S	I_0	I_1	$\overline{Z}$
H	X	X	X	Z
L	H	X	L	H
L	H	X	H	L
L	L	L	X	H
L	L	H	X	L

H = HIGH Voltage Level
L = LOW Voltage Level
X = Immaterial
Z = High Impedance

LOGIC DIAGRAM



DC CHARACTERISTICS OVER OPERATING TEMPERATURE RANGE (unless otherwise specified)

SYMBOL	PARAMETER		54/74S Min	54/74S Max	54/74LS Min	54/74LS Max	UNITS	CONDITIONS
I_{OS}	Output Short Circuit Current		-40	-100	-20	-100	mA	V_{CC} = Max
I_{CC}	Power Supply Current	Outputs HIGH		56		7.0	mA	V_{CC} = Max; S, I_{1x} = 4.5 V $\overline{OE}$, I_{0x} = Gnd
		Outputs LOW		81		14		V_{CC} = Max; I_{1x} = 4.5 V $\overline{OE}$, I_{0x}, S = Gnd
		Outputs OFF		87		19		V_{CC} = Max; S, I_{0x} = Gnd $\overline{OE}$ = I_{1x} = 4.5 V

AC CHARACTERISTICS: V_{CC} = +5.0 V, T_A = +25° C (See Section 3 for waveforms and load configurations)

SYMBOL	PARAMETER	54/74S C_L = 15 pF, R_L = 280 Ω Min	54/74S Max	54/74LS C_L = 15 pF Min	54/74LS Max	UNITS	CONDITIONS
t_{PLH} t_{PHL}	Propagation Delay I_n to $\overline{Z}_n$		6.0 6.0		18 18	ns	Figs. 3-1, 3-4
t_{PLH} t_{PHL}	Propagation Delay S to $\overline{Z}_n$		12 12		21 21	ns	Figs. 3-1, 3-4
t_{PZH} t_{PZL}	Output Enable Time		19.5 21		30 30	ns	Figs. 3-3, 3-11, 3-12 R_L = 2 kΩ ('LS258)
t_{PHZ} t_{PLZ}	Output Disable Time		8.5 14		30 25	ns	Figs. 3-3, 3-11, 3-12 R_L = 2 kΩ, C_L = 5 pF ('LS258)