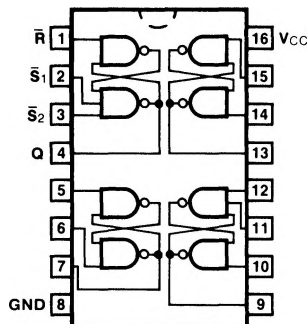


54/74279
54LS/74LS279
 QUAD SET-RESET LATCH

CONNECTION DIAGRAM
PINOUT A



ORDERING CODE: See Section 9

PKGS	PIN OUT	COMMERCIAL GRADE	MILITARY GRADE	PKG TYPE
		$V_{CC} = +5.0\text{ V} \pm 5\%$, $T_A = 0^\circ\text{C to } +70^\circ\text{C}$	$V_{CC} = +5.0\text{ V} \pm 10\%$, $T_A = -55^\circ\text{C to } +125^\circ\text{C}$	
Plastic DIP (P)	A	74279PC, 74LS279PC		9B
Ceramic DIP (D)	A	74279DC, 74LS279DC	54279DM, 54LS279DM	6B
Flatpak (F)	A	74279FC, 74LS279FC	54279FM, 54LS279FM	4L

TRUTH TABLE

INPUTS			OUTPUT Q
\bar{S}_1	\bar{S}_2	\bar{R}	
L	L	L	h
L	X	H	H
X	L	H	H
H	H	L	L
H	H	H	No Change

H = HIGH Voltage Level
 L = LOW Voltage Level
 X = Immaterial
 h = The output is HIGH as long as S_1 or S_2 is LOW. If all inputs go HIGH simultaneously, the output state is indeterminate; otherwise, it follows the Truth Table.

INPUT LOADING/FAN-OUT: See Section 3 for U.L. definitions

PINS	54/74 (U.L.) HIGH/LOW	54/74LS (U.L.) HIGH/LOW
Inputs	1.0/1.0	0.5/0.25
Outputs	20/10	10/5.0 (2.5)

DC AND AC CHARACTERISTICS: See Section 3*

SYMBOL	PARAMETER	54/74		54/74LS		UNITS	CONDITIONS
		Min	Max	Min	Max		
I _{CC}	Power Supply Current	30		7.0		mA	$V_{CC} = \text{Max}, \bar{R} = \text{Gnd}$
t _{PLH} t _{PHL}	Propagation Delay \bar{S} to Q	22 15		22 15		ns	Figs. 3-1, 3-10
t _{PHL}	Propagation Delay \bar{R} to Q	27		27		ns	Figs. 3-1, 3-10

*DC limits apply over operating temperature range; AC limits apply at $T_A = +25^\circ\text{C}$ and $V_{CC} = +5.0\text{ V}$.