

54LS/74LS574

OCTAL D-TYPE FLIP-FLOP

(With 3-State Outputs)

DESCRIPTION — The '574 is a high speed low power octal flip-flop with a buffered common Clock (CP) and a buffered common Output Enable (\overline{OE}). The information presented to the D inputs is stored in the flip-flops on the LOW-to-HIGH Clock (CP) transition.

This device is functionally identical to the 'LS374 except for the pinouts. For complete discussions of operations, truth tables, ac and dc electrical specifications, refer to the 'LS374 data sheet.

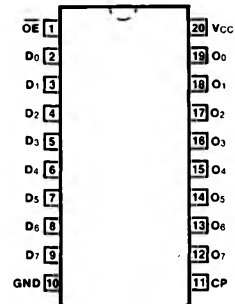
- INPUTS AND OUTPUTS ON OPPOSITE SIDES OF PACKAGE ALLOWING EASY INTERFACE WITH MICROPROCESSORS
- USEFUL AS INPUT OR OUTPUT PORT FOR MICROPROCESSORS
- FUNCTIONALLY IDENTICAL TO 'LS374
- INPUT CLAMP DIODES LIMIT HIGH SPEED TERMINATION EFFECTS
- FULLY TTL AND CMOS COMPATIBLE

ORDERING CODE: See Section 9

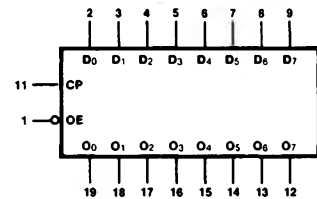
PKGS	PIN OUT	COMMERCIAL GRADE	MILITARY GRADE	PKG TYPE
		$V_{CC} = +5.0\text{ V} \pm 5\%$, $T_A = 0^\circ\text{C to } +70^\circ\text{C}$	$V_{CC} = +5.0\text{ V} \pm 10\%$, $T_A = -55^\circ\text{C to } +125^\circ\text{C}$	
Plastic DIP (P)	A	74LS574PC		9Z
Ceramic DIP (D)	A	74LS574DC	54LS574DM	4E
Flatpak (F)	A	74LS574FC	54LS574FM	4F

CONNECTION DIAGRAM

PINOUT A



LOGIC SYMBOL



V_{CC} = Pin 20
GND = Pin 10

INPUT LOADING/FAN-OUT: See Section 3 for U.L. definitions

PIN NAMES	DESCRIPTION	54/74LS (U.L.) HIGH/LOW
$D_0 - D_7$	Data Inputs	0.5/0.25
CP	Clock Pulse Input (Active Rising Edge)	0.5/0.25
\overline{OE}	3-State Output Enable Input (Active LOW)	0.5/0.25
$O_0 - O_7$	3-State Outputs	65/15 (25)/(7.5)