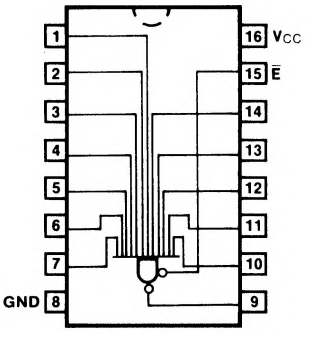
54S/74S134

12-INPUT NAND GATE

(With 3-State Outputs)

CONNECTION DIAGRAM
PINOUT A



ORDERING CODE: See Section 9

PKGS	PIN OUT	COMMERCIAL GRADE V_{CC} = +5.0 V ±5%, T_A = 0° C to +70° C	MILITARY GRADE V_{CC} = +5.0 V ±10%, T_A = -55° C to +125° C	PKG TYPE
Plastic DIP (P)	A	74S134PC		9B
Ceramic DIP (D)	A	74S134DC	54S134DM	6B
Flatpak (F)	A	74S134FC	54S134FM	4L

TRUTH TABLE

INPUTS	OUTPUTS	
A..... L	Enable	Y
H..... H	L	L
Any In LOW	L	H
X..... X	H	Z

H = HIGH Voltage Level
L = LOW Voltage Level
X = Immaterial
Z = High Impedance

INPUT LOADING/FAN-OUT: See Section 3 for U.L. definitions

PINS	54/74S (U.L.) HIGH/LOW
Inputs	1.25/1.25
Outputs	50/12.5

DC AND AC CHARACTERISTICS: See Section 3*

SYMBOL	PARAMETER		54/74S Min	54/74S Max	UNITS	CONDITIONS	
V_{OH}	Output HIGH Voltage	XM	2.4		V	I_{OH} = -2.0 mA	V_{CC} = Min
		XC	2.4			I_{OH} = -6.5 mA	V_{IN} = 0.8 V
I_{CC}	Power Supply Current	Outputs HIGH		13	mA	V_{IN} = 0 V, $V_{\overline{E}}$ = 0 V	V_{CC} = Max
		Outputs LOW		16		V_{IN} = 5.0 V, $V_{\overline{E}}$ = 0 V	
		Outputs OFF		25		V_{IN} = 5.0 V, $V_{\overline{E}}$ = 5.0 V	
t_{PLH} t_{PHL}	Propagation Delay Data to Output		2.0 2.0	6.0 7.5	ns	Figs. 3-3, 3-4	
t_{PZH} t_{PZL}	Output Enable Time			19.5 21	ns	Figs. 3-3, 3-11, 3-12	
t_{PHZ} t_{PLZ}	Output Disable Time			8.5 14	ns	Figs. 3-3, 3-11, 3-12	

*DC limits apply over operating temperature range; AC limits apply at T_A = +25° C and V_{CC} = +5.0 V.