MOTOROLA

Chip Errata

68340 Integrated Processor with DMA

10/06/95

This errata list applies to the following 68340 mask sets:

Mask	Processing Geometry	Part Number Suffix
1F77J	0.8u	"C"
G67F	0.65u	"E"

The mask set for each part is encoded into the device topside markings - for example, the following markings indicate a device from the 1F77J mask, manufactured in the 2nd week of 1995:

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MC68340FE16C
   1F77J
  QEAQ9502
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The errata are organized by mask set, from oldest to newest, with each errata listed under the last mask set that it applies to. When working with 1D75M silicon, for instance, the errata for all prior revisions do not apply - the errata shown for 1D75M and later do apply (unless otherwise specifically noted). The above mask list does not include masks which were never released to production or sampled.

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1F77J

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1. SIM: Autovectored IACK and BR: If BR is asserted during an autovectored IACK cycle, AS will negate 1/2 clock early.
Workaround: Decode the IACK address range (A19 & FC2 & FC1 & FC0 & !AS) and use the resulting signal to force BR high during IACK cycles.

2. SIM: Show Cycles and BR: If show cycles and external arbitration are enabled, and BR is asserted immediately before the clock edge from which DS asserts for a show cycle, the show cycle will be truncated. The data bus drive time for the show cycle will overlap the front end of the alternate master bus tenure by one clock (data will tristate from the clock falling edge one clock after the falling edge BG asserts from).
Workarounds: 1) Disable show cycles when alternate master bus activity is possible. 2) Delay BG assertion to the system by one clock, or delay the alternate master from driving the data bus for one clock after BG asserts.

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G67F

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1. SIM: Loss of Crystal without Limp Mode — If a loss of crystal occurs while the VCO is set to a low operating frequency (131 KHz), the part may lock up and not enter limp mode.

2. CPU: System Clock Minimum Frequency — The minimum operating frequency for all clock modes is 100kHz.

3. DMA: DONEx input — If DONEx is recognized asserted before or after the DACKx signal has been asserted or negated, respectively, the channel will block further recognition of DREQx, but will not clear the STR bit in the DMACCR register or set any of the channel termination status bits in the DMACSR register. This specific device functionality is not guaranteed, and may change on future mask sets.
Workarounds:
a) Assert DONEx after DACKx has been asserted and before DACKx is negated.
b) Since DONEx as an input is used to signal that the current DMA transfer is the last, peripheral devices that signal a done termination when there are no more DMA transfers required can either initiate a dummy DMA transfer with DONEx asserted, or generate an interrupt directly to the CPU. For the direct interrupt, the interrupt service routine can then clear the DMA channel and initialize it for the next transfer.

4. Clock skew for external clock with PLL mode — The MC68340 electrical specifications list a maximum 5ns skew between EXTAL and CLKOUT for external clock with PLL mode. Skew between these 2 edges may exceed +/-5ns. For operating frequencies >= 10MHz, the EXTAL to CLKOUT skew is +9/-5ns maximum (CLKOUT falling edge may occur between 5ns before and 9ns after the corresponding EXTAL falling edge). For frequencies less than 10MHz, the maximum skew is +/-10ns. Note that the PLL locks falling edges (not rising) of the EXTAL clock input and CLKOUT.

NOTES

These notes describe silicon operation which is different from the original documented operation of the 68340. These are permanent features - future documentation revisions will reflect this operation.

1. JTAG, DONEx — The JTAG dma.ctl scan bit (bit #83) documented in the original User's Manual and implemented in silicon revisions through D75M is extraneous and IEEE 1149.1 non-compliant. Silicon revisions after xD75M do not support this bit and all subsequent bits are shifted forward one position. Rev. 1 of the User's Manual documents the revised (D97R and later) JTAG scan chain.

2. PIT, Background Mode — If Background Debug Mode is entered and exited while the PIT is running and the FRZ1 bit in the SIM MCR is set, the PIT value may decrement by an extra count, shortening the timeout period. This will typically only affect emulation.

3. VCCSYN Power — VCCSYN provides power to the VCC pin when the part is powered down. Power VCCSYN from the same supply as VCC, with appropriate filtering as shown in the manual.

4. Serial: RTS operation — In the hardware flow-control mode of operation, the first assertion of RTSx* after enabling the RxRTS bit (MR1 register bit 7) does not have to be done manually. If a FIFO position is available, RTSx* is enabled immediately when the RxRTS bit is set.

5. Serial Transmitter Disabling: The character in the temporary holding register will be lost if the transmitter is disabled. Wait for TxRDY before disabling the transmitter.

6. Recognition of DONEx* as an input during single address transfers has been modified to cause channel termination after the current transfer. Previous silicon would typically run another transfer, but could also stop after the current transfer if the channel was forced off the bus by interrupt activity or other bus masters (2nd DMA channel or external bus request). Effective mask: F77J (rev C).

7. The tDICL (min.) specification #27 has been changed from 5ns (min.) to 8ns (min.) on the MC68340FE16VC, MC68340RP16VC, and MC68340PV16VC only. Effective mask: F77J (rev C).

8. The PLL lock counter has been modified for external clock with VCO mode to increase the clock delay to lock from 328 to 1864 clocks. This delay applies to PLL locking for both power-on reset and exit from LPSTOP (if the VCO was turned off). This means that power-up reset will be slightly longer, and that the SLOCK bit in the SYNCR register will be set slightly later following a reset. Effective mask: F77J (rev C).

9. The appearance of CLKOUT following RESET has been changed if the VCO was turned off during LPSTOP. If CLKOUT was turned off during LPSTOP, it will not resume toggling upon exiting LPSTOP until the PLL has achieved lock. If CLKOUT was selected to be the EXTAL input during LPSTOP, it will not switch back to the VCO output upon exiting LPSTOP until the PLL has achieved lock. These changes affect both crystal and direct-drive mode. All clock switches will still be clean (no short duration highs/lows). Effective mask: F77J (rev C).

10. JTAG I/O control change. Following JTAG test reset (not functional reset), all I/O and output pins will be set to input or high-impedance states. This was not previously true for some pins. Note that most automated vector generators (and most programmers) don't rely on the reset to determine their direction anyway. Effective mask: F77J (rev C).

11. CPU minimum frequency requirements for using the serial module baudrate generator have been relaxed. This means that customers can run the device below 8MHz for baud rates below 76.8K baud. Please refer to the attached description for more detailed information. Effective mask: F77J (rev C).

Serial Module Clocking Change
Preliminary Information

Note: This document contains preliminary information on a functional improvement for the serial module implemented in the 68340 beginning with the F77J mask. The relaxed clock specifications shown are preliminary, and subject to change.

Change description:
The serial module internal clock synchronization has been revised to relax CLKOUT minimum frequency requirements when using the internal baud rate generators. The revised CLKOUT requirements are a relaxation of the current specifications - no change to existing designs will be required to accommodate this feature.

Previously, a minimum 8.3MHz CLKOUT frequency was required to use the internal baud rate generators with the default 3.6864MHz serial crystal. In the new serial module, the serial clock synchronization has been modified to allow the minimum CLKOUT frequency to be scaled depending on the maximum baud rate selected. Operation and specifications for external clocking via SCLK are not affected by this change.

Table 1 below shows the resulting minimum CLKOUT frequency for each programmable baud rate. Note that applications using the VCO clock modes - crystal and external clock with VCO - are restricted to a 131KHz minimum CLKOUT frequency. An errata exists which also limits CLKOUT to 100KHz for external clock without VCO mode; refer to the silicon errata for each part.

baud rate	CLKOUT Fmin	baud rate	CLKOUT Fmin
50	3250Hz*	1800	116kHz*
75	4850Hz*	2000	129kHz*
110	7090Hz*	2400	154kHz
134.5	8660Hz*	4800	309kHz
150	9650Hz*	7200	465kHz
200	12.9kHz*	9600	621kHz
300	19.3kHz*	19200	1.26MHz
600	38.5kHz*	38400	2.56MHz
1050	67.3kHz*	76800	8.29MHz
1200	76.9kHz*		

*Note: See text for other minimum system frequency considerations

Table 1: Minimum CLKOUT Frequency vs. Baud Rate

The minimum CLKOUT frequency is calculated using the following formula:

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CLKOUT(min) = 1/((1/(baud_rate*sample_rate)-Tsetup-Thold)/2)
            = (50-38400 baud):  1/((1/(baud_rate*32)-30ns)/2)
                    or
              (76.8K baud):     1/((1/(baud_rate*48)-30ns)/2)
Tsetup+Thold = 30ns
Sample_rate = 48 for 76.8Kbaud, 32 for others
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Note that with this revision, replacing the serial crystal with a lower subfrequency (1.8432MHz for example) no longer affects the minimum CLKOUT frequency for a specific baud rate, since the selected baud clock is now synchronized. Also, the logic for the CTSx inputs uses the 1200baud clock as a sample clock - CLKOUT Fmin should be kept above 76.9KHz to avoid affecting CTSx sampling.

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