DEVICE ERRATA

February 20, 1997

68EN302 INTEGRATED MULTIPROTOCOL PROCESSOR DEVICE

This document covers the XC68EN302 Mask 1H56B (Rev A). Errata listed in italics and which have change bars are new since the last published errata.

1. Potential for zero-length filled buffers on receive.

In normal operation, the L (last) bit is set in the last buffer descriptor of received frames. A special set of conditions exists where an extra receive buffer will be utilized (with L=1) whose length field will be set to zero. The condition: 1) Frame length is an integral number of buffers, 2) “dribble bits” must have been received with the frame, 3) The Burst Limit (BLIM) must be set higher than the watermark (WMRK), and 4) bus access latency must be “short” (i.e. the bu must be readily available).

Workaround: Software drivers should deal with zero-length filled buffers. The buffer descriptor will contain the frame status bits.

This bug exists in Rev0.1 (1G97C) and Rev. A.1 (1H56B). A fix has not been scheduled for this bug.

2. 68302 timing exceptions (Specifications 5a, 27, 47)

The following 68302 timing specifications are not met by the 68EN302:

68302 Timing Specification	68302 @ 25 MHz	EN302 @ 25 MHz
5A - EXTAL to CLKO delay	9 ns*	9 ns
27 - DATA in to CLKO low setup	5 ns	10 ns
47 - Async Input setup	7 ns	12 ns

* An errata has been issued for 68302 specification 5A changing it from 7 ns max to 9 ns max at 25MHz. The changed 9ns max is met by Rev A.1 silicon.

3. MBC State Machine (MBC_SM) Hangs when DTACK not Returned

If a read or write to a module bus location occurs that does not return mtab(DTACK), the MBC_SM hangs in the s4_mb state until the next module bus transaction occurs. Examples of locations that don't return DTACK are unimplemented registers, and BDRAM or AR RAM when ETHER_EN is deasserted.

WORKAROUND: Do not read or write to locations that are not meant to be read or written. Once software is debugged, this problem should not be encountered.

This bug exists in Rev 0.1 (1G97C) thru Rev A.1 (1H56B) silicon. A fix is planned for Rev. B silicon.

4. Use of Wrap bit in Ethernet Receive Buffer Descriptors (RX BD).

Setting the Wrap bit (W bit is bit 13 in the first word of an RX BD) in the Ethernet Receive buffer descriptors does not work properly except in a subset of the possible receive buffer descriptors. Setting the Wrap bit in any of the first 8 receive buffer descriptors will result in correct wrapping back to the initial receive buffer descriptor. After the first 8 buffer descriptors, wrapping works correctly in every 8th buffer descriptor.

WORKAROUNDS:

1. Don't use the Wrap bit in receive buffer descriptors
2. Only use the Wrap bit in one of the first 8 or thereafter in a multiple of 8 receive buffer descriptors.

This bug exists in Rev 0.1 (1G97C) and Rev A.1 (1H56B) silicon. A fix is planned for Rev. B silicon.

5. Address Recognition

A.) PA_REJ Control Bit

Setting the PA_REJ bit in the AR_CNTRL register is supposed to invert the result of address recognition on unicast (physical) addresses. When PA_REJ = 1, a perfect match will result in the frame being rejected; if no match occurs, the frame should be received. What actually happens is all unicast frames are rejected when PA_REJ is set and HASH_EN is zero.

WORKAROUND: The PA_REJ function does work if HASH_EN is set = 1. If the hash table address recognition function is not wanted, then set HASH_EN = 1 and load the hash table with all zeros. This reduces the AR RAM from 64 entries to 62 entries. The 64-bit hash table is located at the following four locations:

MOBA + $BF0
MOBA + $BF2
MOBA + $BF8
MOBA + $BFA

Refer to sections 4.1.9 (AR CONTROL REGISTER) and 4.6 (Address Recognition) of the MC68EN302 Reference Manual for a detailed description of the address recognition function.

This bug exists in Rev 0.1 (1G97C) and Rev A.1 (1H56B) silicon. A fix is planned for Rev. B silicon.

B.) Address Recognition - Hash Match in Progress when Software Write to AR RAM Occurs.

If hashmode is used, AND an incoming frame does not match any perfect-match entry, AND is about to do the hash check but the AR RAM is being written to/read from during that clock cycle, then there is a possibility (if hash bits 4 and 5 are different which is frame destination address dependent) of checking against the wrong bit in the hash table. Depending on the hash table entry values pointed to then the frame MAY be incorrectly accepted or rejected.

This bug exists in Rev 0.1 (1G97C) and Rev A.1 (1H56B) silicon. A fix is planned for Rev. B silicon.

6. Vih/Vil Sensitivity

The following pins have out of spec Vih/Vil behavior:

TRST (JTAG Reset pin)
Vih Min = 3.4 V

TCLK (Ethernet Transmit Clock)
Vih Min = 2.8 V
Vil Max = 0.4 V

This bug exists in Rev 0.1 (1G97C) and Rev A.1 (1H56B) silicon. The fix is under investigation.

7. Failure to Close a Transmit Buffer Descriptor Following Excessive or Late Collisions.

Following a transmission which encounters either excessive collisions or a late collision, the corresponding transmit buffer descriptor may not be closed by hardware. This failure to close the transmit buffer descriptor will occur only if receive activity is present when the buffer descriptor would normally be closed.

If this happens as an isolated incident, closing of buffer descriptors will resume with the next frame; however, status will be reported on buffer descriptor #n-1 for frame #n (assuming single buffer frames). If this happens on two consecutive transmit frames, the transmit DMA buffer descriptor control logic will lock up and no additional frames will be transmitted.

WORKAROUND: The only known workaround for the transmit lockup condition is to detect this condition with a software controlled timer and reinitialize the Ethernet logic (deassert ETHER_EN, reinitialize buffer descriptors reassert ETHER_EN).

This bug exists in Rev 0.1 (1G97C) thru Rev A.1 (1H56B) silicon. A fix is planned for Rev. B silicon.

8. CSL, DEF bits in Transmit Buffer Descriptor may Incorrectly Set on Frame with LC or RL bits Set.

On transmit frames which encounter either a late collision or excessive collisions, the CSL and DEF bits in the transmit buffer descriptor MAY also be set. These status bits should not be set for frames which encounter collisions. These status bits in the transmit buffer descriptor do not impact operation, but are used for incrementing optional software counters to provide network management status.

WORKAROUND: If software implements the recommended "Number of Carrier Sense Errors" counter as defined in the 802.3 standard, this counter should only be incremented if CSL = 1 and LC = RL = 0. If software implements the recommended "Number of frames with deferred transmission" counter as defined in the 802.3 standard, this counter should only be incremented if CSL = 1 and LC = RL = 0.

This bug exists in Rev 0.1 (1G97C) thru Rev A.1 (1H56B) silicon. A fix is planned for Rev B silicon.

9. Receive FIFO Overflow Condition, Frame Counter in Receive FIFO Control Logic.

If a receive FIFO overflow condition occurs, the receive FIFO control logic may incorrectly count the number of frames in the receive FIFO. This can occur if software provides buffer descriptors with the Empty bit = 1, allowing the DMA engine to empty the receive FIFO after the overflow has occured. If the receive FIFO is emptied while a receive frame is present on the network, the internal frame count may become incorrect. After this happens, buffer descriptors may be incorrectly written by the DMA engine (Empty bit cleared and status bits written) until the internal frame counter returns to zero.

WORKAROUND: The only known workaround for this condition is to detect incorrect receive buffer descriptors and reinitialize the Ethernet logic (deassert ETHER_EN, reinitialize buffer descriptors, reassert ETHER_EN). An incorrect receive buffer desciptor is one with the L bit set when no corresponding buffer with F bit set has occured.

This bug exists in Rev 0.1 (1G97C) thru Rev A.1 (1H56B) silicon. A fix is planned for Rev. B silicon.