

May 1992 Revised November 1999

74ABT2244

Octal Buffer/Line Driver with 25 Ω Series Resistors in the Outputs

General Description

The ABT2244 is an octal buffer and line driver designed to drive the capacitive inputs of MOS memory drivers, address drivers, clock drivers, and bus-oriented transmitters/receivers.

The 25Ω series resistors in the outputs reduce ringing and eliminate the need for external resistors.

Features

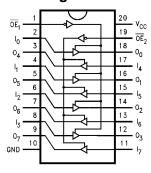
- Guaranteed latchup protection
- High impedance glitch-free bus loading during entire power up and power down cycle
- Nondestructive hot insertion capability

Ordering Code:

Order Number	Package Number	Package Description			
74ABT2244CSC	M20B	20-Lead Small Outline Integrated Circuit (SOIC), JEDEC MS-013, 0.300" Wide Body			
74ABT2244CSJ	M20D	20-Lead Small Outline Package (SOP), EIAJ TYPE II, 5.3mm Wide			
74ABT2244CMSA	MSA20	20-Lead Shrink Small Outline Package (SSOP), EIAJ TYPE II, 5.3mm Wide			
74ABT2244CMTC	MTC20	20-Lead Thin Shrink Small Outline Package (TSSOP), JEDEC MO-153, 4.4mm Wide			
74ABT2244CPC	N20A	20-Lead Plastic Dual-In-Line Package (PDIP), JEDEC MS-001, 0.300" Wide			

Devices are also available in Tape and Reel. Specify by appending the suffix letter "X" to the ordering code.

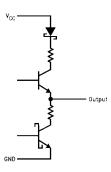
Connection Diagram



Pin Descriptions

Pin Names	Description		
\overline{OE}_1 , \overline{OE}_2	Output Enable Input (Active LOW)		
I ₀ —I ₇	Inputs		
O ₀ –O ₇	Outputs		

Schematic of Each Output



Truth Table

OE ₁	I ₀₋₃	O ₀₋₃	OE ₂	I ₄₋₇	O ₄₋₇
Н	Х	Z	Н	Х	Z
L	Н	Н	L	Н	Н
L	L	L	L	L	L

H = HIGH Voltage Level

L = LOW Voltage Level

X = Immaterial Z = High Impedance

Absolute Maximum Ratings(Note 1)

Recommended Operating Conditions

-65°C to +150°C Storage Temperature -55°C to +125°C Ambient Temperature under Bias

Junction Temperature under Bias -55°C to +150°C V_{CC} Pin Potential to Ground Pin -0.5V to +7.0V

Input Voltage (Note 2) -0.5V to +7.0VInput Current (Note 2) -30 mA to +5.0 mA

Voltage Applied to Any Output

in the Disabled or

Power-off State -0.5V to 5.5Vin the HIGH State -0.5V to V_{CC}

Current Applied to Output

in LOW State (Max) twice the rated I_{OL} (mA)

DC Latchup Source Current

(Across Comm Operating Range) -300 mA

Over Voltage Latchup (I/O) 10V

Free Air Ambient Temperature -40°C to +85°C Supply Voltage +4.5V to +5.5V

Minimum Input Edge Rate (ΔV/Δt)

Data Input 50 mV/ns **Enable Input** 20 mV/ns

Note 1: Absolute maximum ratings are values beyond which the device may be damaged or have its useful life impaired. Functional operation under these conditions is not implied.

DC Electrical Characteristics

Symbol	P	arameter	Min	Тур	Max	Units	v _{cc}	Conditions
V _{IH}	Input HIGH Volt	age	2.0			V		Recognized HIGH Signal
V _{IL}	Input LOW Volta	age			0.8	V		Recognized LOW Signal
V _{CD}	Input Clamp Dic	ode Voltage			-1.2	V	Min	I _{IN} = -18 mA
V _{OH}	Output HIGH		2.5			V	Min	$I_{OH} = -3 \text{ mA}$
			2.0			V	Min	$I_{OH} = -32 \text{ mA}$
V _{OL}	Output LOW Vo	Itage			8.0	V	Min	I _{OL} = 15 mA
I _{IH}	Input HIGH Curi	rent			1		Max	V _{IN} = 2.7V (Note 4)
					1	μА	IVIAX	$V_{IN} = V_{CC}$
I _{BVI}	Input HIGH Curi	rent Breakdown Test			7	μΑ	Max	V _{IN} = 7.0V
I _{IL}	Input LOW Curr	ent			-1	μА	Max	V _{IN} = 0.5V (Note 4)
					-1	μΛ	IVIAX	$V_{IN} = 0.0V$
V _{ID}	Input Leakage T	est	475			V	0.0	$I_{ID} = 1.9 \mu A$
			475			V	0.0	All Other Pins Grounded
I _{OZH}	Output Leakage	Current			10	μΑ	0 – 5.5V	V _{OUT} = 2.7V; OE n = 2.0V
I _{OZL}	Output Leakage Current				-10	μΑ	0 – 5.5V	V _{OUT} = 0.5V; OE n = 2.0V
Ios	Output Short-Ci	rcuit Current	-100		-275	mA	Max	V _{OUT} = 0.0V
I _{CEX}	Output HIGH Le	akage Current			50	μА	Max	$V_{OUT} = V_{CC}$
I _{ZZ}	Bus Drainage Test				100	μΑ	0.0	V _{OUT} = 5.5V; All Others GND
I _{CCH}	Power Supply C	Current			50	μΑ	Max	All Outputs HIGH
I _{CCL}	Power Supply C	Current			30	mA	Max	All Outputs LOW
I _{CCZ}	Power Supply C	Current			50	μΑ	Max	OEn = V _{CC}
								All Others at V _{CC} or GND
I _{CCT}	Additional	Outputs Enabled			2.5	mA		$V_I = V_{CC} - 2.1V$
	I _{CC} /Input	Outputs 3-STATE			2.5	mA	Max	Enable Input V _I = V _{CC} - 2.1V
		Outputs 3-STATE			50	μΑ		Data Input V _I = V _{CC} - 2.1V
								All Others at V _{CC} or GND
I _{CCD}	Dynamic I _{CC}	No Load				mA/	Max	Outputs OPEN
	(Note 4)				0.1	MHz		OEn = GND (Note 3)
								One Bit Toggling, 50% Duty Cycle

Note 2: Either voltage limit or current limit is sufficient to protect inputs.

Note 3: For 8 bits toggling, $I_{CCD} < 0.8 \text{ mA/MHz}.$

Note 4: Guaranteed, but not tested.

AC Electrical Characteristics

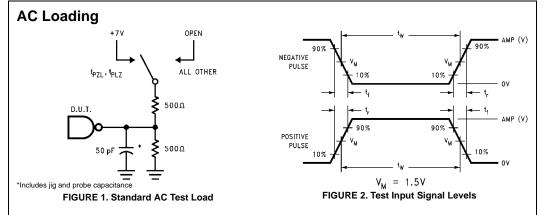
(SOIC and SSOP Package)

Symbol	Parameter	$T_A = +25$ °C $V_{CC} = +5V$ $C_L = 50$ pF			$T_A = -40^{\circ}\text{C to } +85^{\circ}\text{C}$ $V_{CC} = 4.5\text{V} - 5.5\text{V}$ $C_L = 50 \text{ pF}$		Units
		Min	Тур	Max	Min	Max	
t _{PLH}	Propagation	1.0	2.2	3.9	1.0	3.9	
t _{PHL}	Delay Data to Outputs	1.0	2.9	4.4	1.0	4.4	ns
t _{PZH}	Output Enable	1.5	3.7	6.0	1.5	6.0	
t_{PZL}	Time	2.1	4.3	7.0	2.1	7.0	ns
t _{PHZ}	Output Disable	1.7	3.5	5.8	1.7	5.8	ns
t_{PLZ}	Time	1.7	3.7	5.8	1.7	5.8	115

Capacitance

Sy	mbol	Parameter	Тур	Units	Conditions T _A = 25°C
C _{IN}		Input Capacitance	5.0	pF	V _{CC} = 0V
C _{OUT} (N	Note 5)	Output Capacitance	9.0	pF	V _{CC} = 5.0V

Note 5: C_{OUT} is measured at frequency f = 1 MHz, per MIL-STD-883, Method 3012.



Amplitude	Rep. Rate	t _w	t _r	t _f
3.0V	1 MHz	500 ns	2.5 ns	2.5 ns

FIGURE 3. Test Input Signal Requirements

AC Waveforms

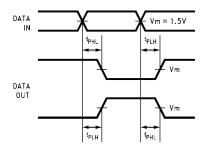


FIGURE 4. Propagation Delay Waveforms for Inverting and Non-Inverting Functions

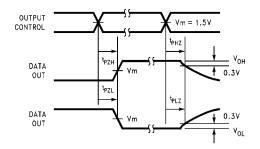


FIGURE 5. 3-STATE Output HIGH and LOW Enable and Disable Times

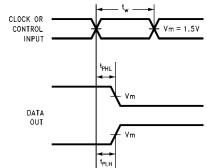


FIGURE 6. Propagation Delay, Pulse Width Waveforms

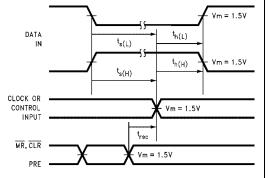
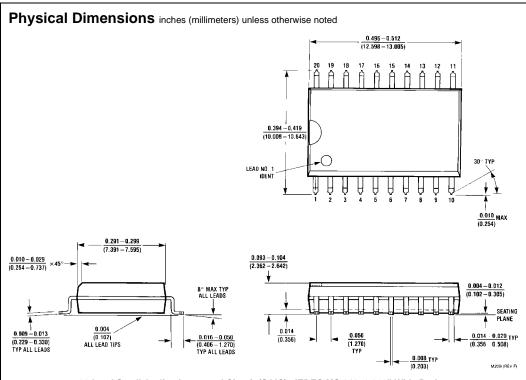
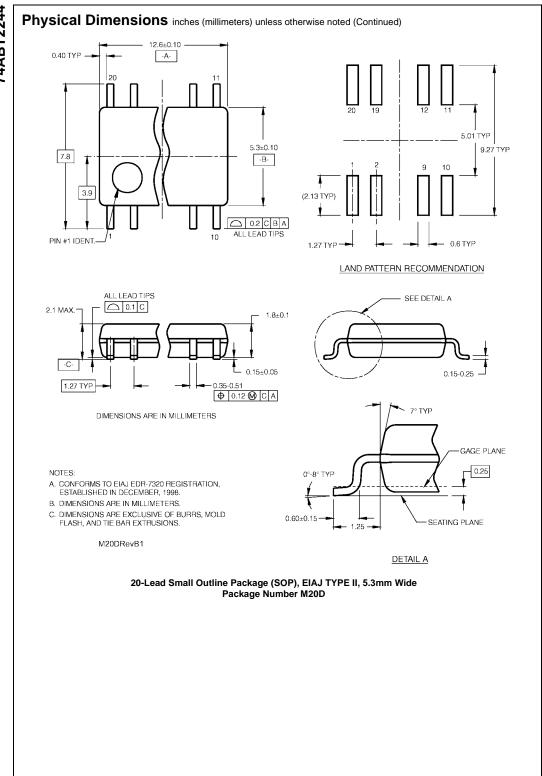
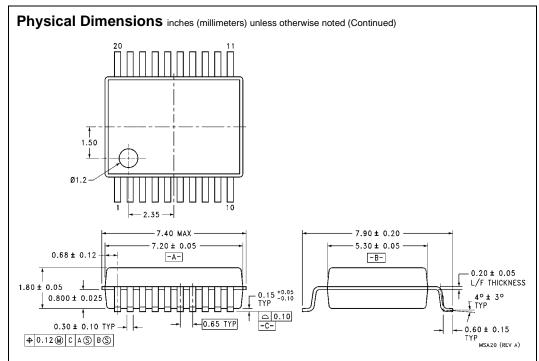


FIGURE 7. Setup Time, Hold Time and Recovery Time Waveforms

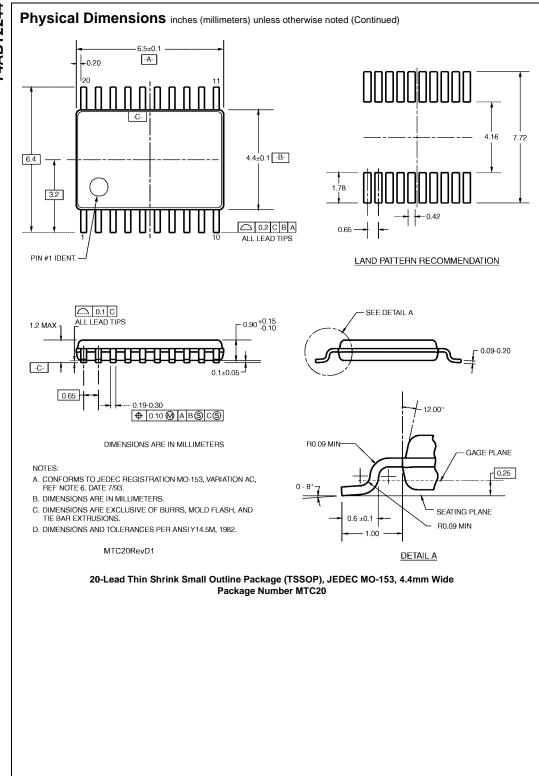


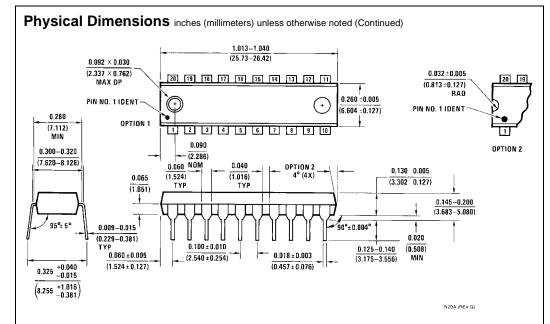
20-Lead Small Outline Integrated Circuit (SOIC), JEDEC MS-013, 0.300" Wide Body Package Number M20B





20-Lead Shrink Small Outline Package (SSOP), EIAJ TYPE II, 5.3mm Wide Package Number MSA20





20-Lead Plastic Dual-In-Line Package (PDIP), JEDEC MS-001, 0.300" Wide Package Number N20A

Fairchild does not assume any responsibility for use of any circuitry described, no circuit patent licenses are implied and Fairchild reserves the right at any time without notice to change said circuitry and specifications.

LIFE SUPPORT POLICY

FAIRCHILD'S PRODUCTS ARE NOT AUTHORIZED FOR USE AS CRITICAL COMPONENTS IN LIFE SUPPORT DEVICES OR SYSTEMS WITHOUT THE EXPRESS WRITTEN APPROVAL OF THE PRESIDENT OF FAIRCHILD SEMICONDUCTOR CORPORATION. As used herein:

- Life support devices or systems are devices or systems which, (a) are intended for surgical implant into the body, or (b) support or sustain life, and (c) whose failure to perform when properly used in accordance with instructions for use provided in the labeling, can be reasonably expected to result in a significant injury to the user.
- A critical component in any component of a life support device or system whose failure to perform can be reasonably expected to cause the failure of the life support device or system, or to affect its safety or effectiveness.

www.fairchildsemi.com