INTEGRATED CIRCUITS

DATA SHEET

74ABT32Quad 2-input OR gate

Product specification

1995 Sep 22

IC23 Data Handbook





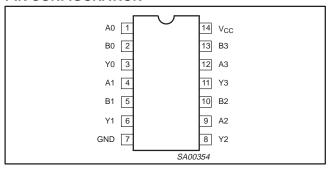
Quad 2-input OR gate

74ABT32

QUICK REFERENCE DATA

SYMBOL	PARAMETER	CONDITIONS T _{amb} = 25°C; GND = 0V	TYPICAL	UNIT
t _{PLH} t _{PHL}	Propagation delay An, Bn to Yn	C _L = 50pF; V _{CC} = 5V	2.3 1.9	ns
toslh toshl	Output to Output skew	ACC = 2A	0.4	ns
C _{IN}	Input capacitance	$V_I = 0V \text{ or } V_{CC}$	3	pF
I _{CC}	Total supply outputs disabled; V _{CC} = 5.5V		50	μΑ

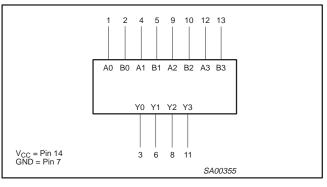
PIN CONFIGURATION



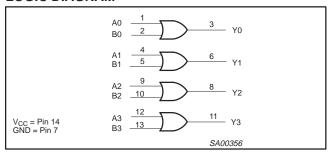
PIN DESCRIPTION

PIN NUMBER	SYMBOL	NAME AND FUNCTION
1, 2, 4, 5, 9, 10, 12, 13	An, Bn	Data inputs
3, 6, 8, 11	Yn	Data outputs
7	GND	Ground (0V)
14	V _{CC}	Positive supply voltage

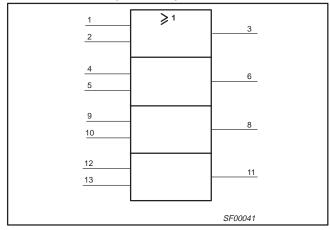
LOGIC SYMBOL



LOGIC DIAGRAM



LOGIC SYMBOL (IEEE/IEC)



FUNCTION TABLE

INP	JTS	OUTPUT				
An	Bn	Yn				
L	L	L				
L	Н	Н				
Н	L	Н				
Н	Н	Н				

NOTES:

H = High voltage level L = Low voltage level

ORDERING INFORMATION

ONDERNING IN ORMATION				
PACKAGES	TEMPERATURE RANGE	OUTSIDE NORTH AMERICA	NORTH AMERICA	DWG NUMBER
14-Pin Plastic DIP	-40°C to +85°C	74ABT32 N	74ABT32 N	SOT27-1
14-Pin plastic SO	-40°C to +85°C	74ABT32 D	74ABT32 D	SOT108-1
14-Pin Plastic SSOP Type II	-40°C to +85°C	74ABT32 DB	74ABT32 DB	SOT337-1
14-Pin Plastic TSSOP Type I	-40°C to +85°C	74ABT32 PW	74ABT32PW DH	SOT402-1

Quad 2-input OR gate

74ABT32

ABSOLUTE MAXIMUM RATINGS^{1, 2}

SYMBOL	PARAMETER	CONDITIONS	RATING	UNIT
V _{CC}	DC supply voltage		-0.5 to +7.0	V
I _{IK}	DC input diode current	V _I < 0	-18	mA
V _I	DC input voltage ³		-1.2 to +7.0	V
I _{OK}	DC output diode current	V _O < 0	-50	mA
V _{OUT}	DC output voltage ³	output in Off or High state	-0.5 to +5.5	V
I _{OUT}	DC output current	output in Low state	40	mA
T _{stg}	Storage temperature range		-65 to 150	°C

NOTES

- 1. Stresses beyond those listed may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
- 2. The performance capability of a high-performance integrated circuit in conjunction with its thermal environment can create junction temperatures which are detrimental to reliability. The maximum junction temperature of this integrated circuit should not exceed 150°C.
- 3. The input and output voltage ratings may be exceeded if the input and output current ratings are observed.

RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER	LIM	ITS	UNIT
STWIBOL	FARAMETER	MIN	MAX	ONIT
V _{CC}	DC supply voltage	4.5	5.5	V
VI	Input voltage	0	V _{CC}	V
V _{IH}	High-level input voltage	2.0		V
V _{IL}	Low-level input voltage		0.8	V
I _{OH}	High-level output current		–15	mA
I _{OL}	Low-level output current		20	mA
Δt/Δν	Input transition rise or fall rate	0	10	ns/V
T _{amb}	Operating free-air temperature range	-40	+85	°C

DC ELECTRICAL CHARACTERISTICS

					LIMITS			
SYMBOL	PARAMETER	TEST CONDITIONS	Tai	_{nb} = +25	s∘ C	T _{amb} =	UNIT	
			MIN	TYP	MAX	MIN	MAX	1
V _{IK}	Input clamp voltage	$V_{CC} = 4.5V; I_{IK} = -18mA$		-0.9	-1.2		-1.2	V
V _{OH}	High-level output voltage	$V_{CC} = 4.5V$; $I_{OH} = -15mA$; $V_I = V_{IL}$ or V_{IH}	2.5	2.9		2.5		V
V _{OL}	Low-level output voltage	$V_{CC} = 4.5V$; $I_{OL} = 20mA$; $V_I = V_{IL}$ or V_{IH}		0.35	0.5		0.5	V
I _I	Input leakage current	$V_{CC} = 5.5V; V_{I} = GND \text{ or } 5.5V$		±0.01	±1.0		±1.0	μΑ
I _{OFF}	Power-off leakage current	$V_{CC} = 0.0V$; V_O or $V_I \le 4.5V$		±5.0	±100		±100	μΑ
I _{CEX}	Output High leakage current	$V_{CC} = 5.5V$; $V_O = 5.5V$; $V_I = GND$ or V_{CC}		5.0	50		50	μΑ
Io	Output current ¹	$V_{CC} = 5.5V; V_{O} = 2.5V$	-50	-75	-180	-50	-180	mA
I _{CC}	Quiescent supply current	$V_{CC} = 5.5V$; $V_I = GND$ or V_{CC}		2	50		50	μΑ
Δl _{CC}	Additional supply current per input pin ²	V_{CC} = 5.5V; One data input at 3.4V, other inputs at V_{CC} or GND		0.25	500		500	μА

NOTES:

- 1. Not more than one output should be tested at a time, and the duration of the test should not exceed one second.
- 2. This is the increase in supply current for each input at 3.4V.
- 3. For valid test results, data must not be loaded into the flip-flop or latch after applying the power.

1995 Sep 22

AC CHARACTERISTICS

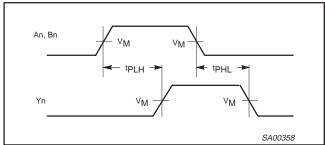
GND = 0V; t_R = t_F = 2.5ns; C_L = 50pF, R_L = 500 Ω

SYMBOL	PARAMETER	WAVEFORM	T _a	_{imb} = +25° 'CC = +5.0'	C V	T _{amb} = -40° V _{CC} = +5.	UNIT	
			MIN	TYP	MAX	MIN	MAX	
t _{PLH}	Propagation delay An, Bn to Yn	1	1.0 1.0	2.3 1.9	3.4 2.9	1.0 1.0	3.8 3.2	ns
toshL toshh1	Output to Output skew An or Bn to \overline{Y} n			0.4	0.5		0.5	ns

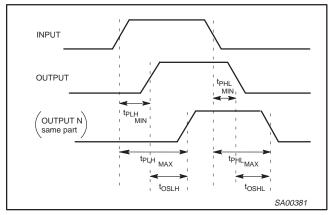
NOTE:

AC WAVEFORMS

 $V_{M} = 1.5V, V_{IN} = GND \text{ to } 3.0V$

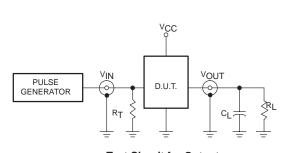


Waveform 1. Propagation delay for inverting outputs



Waveform 2. Common edge skew

TEST CIRCUIT AND WAVEFORMS



Test Circuit for Outputs

AMP (V) 90% **NEGATIVE** ^{V}M PULSE 10% 10% t_{TLH} (t_{R}) tTHL (tF) tTLH (tR) tTHL (tF) AMP (V) 90% 90% POSITIVE PULSE 10% $V_{M} = 1.5V$

Input Pulse Definition

FAMILY	IN	INPUT PULSE REQUIREMENTS											
PAWILI	Amplitude	Rep. Rate	t _W	t _R	t _F								
74ABT	3.0V	1MHz	500ns	2.5ns	2.5ns								

DEFINITIONS

R_L = Load resistor; see AC CHARACTERISTICS for value.

C_L = Load capacitance includes jig and probe capacitance; see AC CHARACTERISTICS for value.

Termination resistance should be equal to Z_{OUT} of pulse generators.

1995 Sep 22

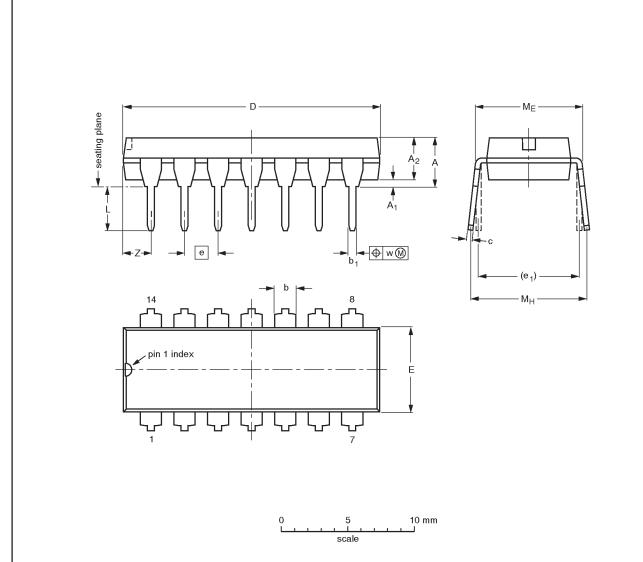
Skew is defined as the absolute value of the difference between the actual propagation delay for any two separate outputs of the same device. The specification applies to any outputs switching in the the same direction, either HIGH-to-LOW (t_{OSHL}) or LOW-to-HIGH (t_{OSLH}); parameter guaranteed by design.

Quad 2-input OR gate

74ABT32

DIP14: plastic dual in-line package; 14 leads (300 mil)

SOT27-1



DIMENSIONS (inch dimensions are derived from the original mm dimensions)

UNIT	A max.	A ₁ min.	A ₂ max.	b	b ₁	С	D ⁽¹⁾	E ⁽¹⁾	е	e ₁	L	ME	M _H	w	Z ⁽¹⁾ max.
mm	4.2	0.51	3.2	1.73 1.13	0.53 0.38	0.36 0.23	19.50 18.55	6.48 6.20	2.54	7.62	3.60 3.05	8.25 7.80	10.0 8.3	0.254	2.2
inches	0.17	0.020	0.13	0.068 0.044	0.021 0.015	0.014 0.009	0.77 0.73	0.26 0.24	0.10	0.30	0.14 0.12	0.32 0.31	0.39 0.33	0.01	0.087

Note

1. Plastic or metal protrusions of 0.25 mm maximum per side are not included.

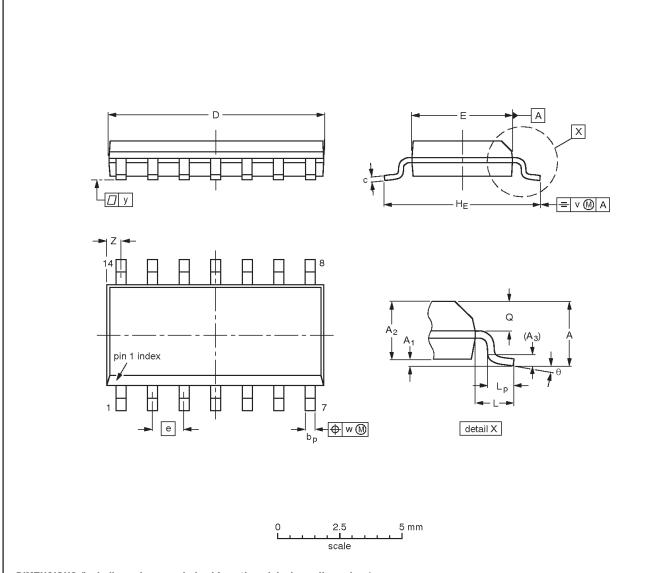
OUTLINE		REFER	EUROPEAN	ISSUE DATE		
VERSION	IEC	JEDEC	EIAJ	PROJECTION	ISSUE DATE	
SOT27-1	050G04	MO-001AA			92-11-17 95-03-11	

Quad 2-input OR gate

74ABT32

SO14: plastic small outline package; 14 leads; body width 3.9 mm

SOT108-1



DIMENSIONS (inch dimensions are derived from the original mm dimensions)

UNIT	A max.	A ₁	A ₂	A ₃	bp	С	D ⁽¹⁾	E ⁽¹⁾	е	HE	L	Lp	Q	v	w	у	Z ⁽¹⁾	θ
mm	1.75	0.25 0.10	1.45 1.25	0.25	0.49 0.36	0.25 0.19	8.75 8.55	4.0 3.8	1.27	6.2 5.8	1.05	1.0 0.4	0.7 0.6	0.25	0.25	0.1	0.7 0.3	8°
inches	0.069	0.010 0.004	0.057 0.049	0.01		0.0100 0.0075		0.16 0.15	0.050	0.244 0.228	0.041	0.039 0.016	0.028 0.024	0.01	0.01	0.004	0.028 0.012	0°

Note

1. Plastic or metal protrusions of 0.15 mm maximum per side are not included.

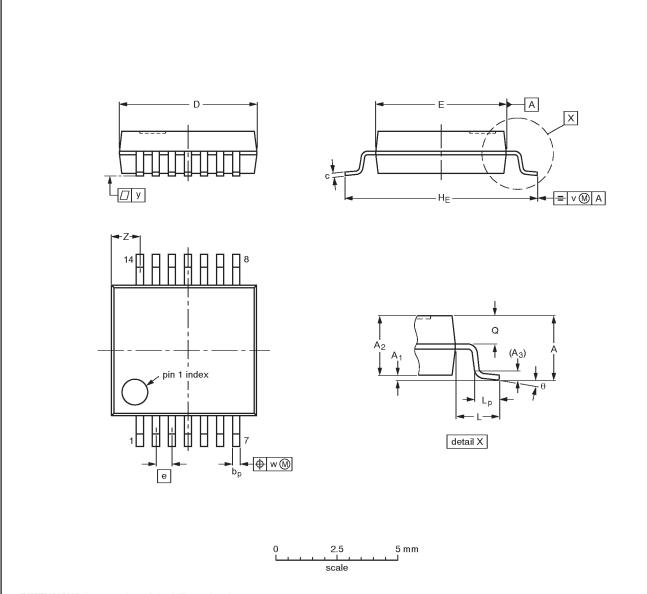
OUTLINE		EUROPEAN	ISSUE DATE				
VERSION	IEC	JEDEC	EIAJ		PROJECTION	ISSUE DATE	
SOT108-1	076E06S	MS-012AB				95-01-23 97-05-22	

Quad 2-input OR gate

74ABT32

SSOP14: plastic shrink small outline package; 14 leads; body width 5.3 mm

SOT337-1



DIMENSIONS (mm are the original dimensions)

UNIT	A max.	A ₁	A ₂	A ₃	bp	c	D ⁽¹⁾	E ⁽¹⁾	е	HE	L	Lp	Q	v	w	у	Z ⁽¹⁾	θ
mm	2.0	0.21 0.05	1.80 1.65	0.25	0.38 0.25	0.20 0.09	6.4 6.0	5.4 5.2	0.65	7.9 7.6	1.25	1.03 0.63	0.9 0.7	0.2	0.13	0.1	1.4 0.9	8° 0°

Note

1. Plastic or metal protrusions of 0.25 mm maximum per side are not included.

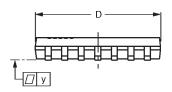
OUTLINE		REFER	EUROPEAN	ISSUE DATE			
VERSION	IEC	JEDEC	EIAJ		PROJECTION	ISSUE DATE	
SOT337-1		MO-150AB				-95-02-04 96-01-18	

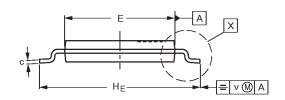
Quad 2-input OR gate

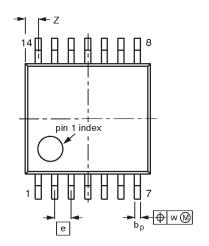
74ABT32

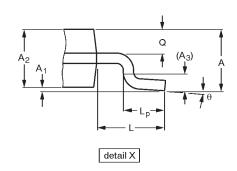
TSSOP14: plastic thin shrink small outline package; 14 leads; body width 4.4 mm

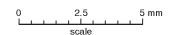
SOT402-1











DIMENSIONS (mm are the original dimensions)

UNIT	A max.	Α1	A ₂	A ₃	bр	c	D ⁽¹⁾	E ⁽²⁾	е	HE	L	Lp	Q	v	w	у	Z ⁽¹⁾	θ
mm	1.10	0.15 0.05	0.95 0.80	0.25	0.30 0.19	0.2 0.1	5.1 4.9	4.5 4.3	0.65	6.6 6.2	1.0	0.75 0.50	0.4 0.3	0.2	0.13	0.1	0.72 0.38	8° 0°

Notes

- 1. Plastic or metal protrusions of 0.15 mm maximum per side are not included.
- 2. Plastic interlead protrusions of 0.25 mm maximum per side are not included.

OUTLINE		EUROPEAN	ISSUE DATE				
VERSION	IEC	JEDEC	EIAJ		PROJECTION	ISSUE DATE	
SOT402-1		MO-153				94-07-12 95-04-04	

Quad 2-input OR gate

74ABT32

NOTES

Quad 2-input OR gate

74ABT32

	DEFINITIONS						
Data Sheet Identification	Product Status	Definition					
Objective Specification	Formative or in Design	This data sheet contains the design target or goal specifications for product development. Specifications may change in any manner without notice.					
Preliminary Specification	Preproduction Product	This data sheet contains preliminary data, and supplementary data will be published at a later date. Philips Semiconductors reserves the right to make changes at any time without notice in order to improve design and supply the best possible product.					
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