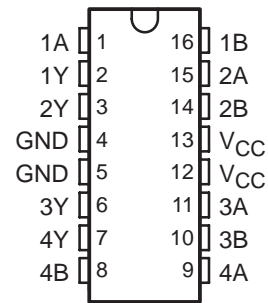


74ACT11086 QUADRUPLE 2-INPUT EXCLUSIVE-OR GATE

SCAS091 – D3990, NOVEMBER 1989 – REVISED APRIL 1993

- Inputs Are TTL-Voltage Compatible
- Flow-Through Architecture Optimizes PCB Layout
- Center-Pin V_{CC} and GND Configurations Minimize High-Speed Switching Noise
- EPIC™ (Enhanced-Performance Implanted CMOS) 1- μ m Process
- 500-mA Typical Latch-Up Immunity at 125°C
- Package Options Include Plastic Small-Outline Packages and Standard Plastic 300-mil DIPs

D OR N PACKAGE
(TOP VIEW)



description

This device contains four independent 2-input exclusive-OR gates. They perform the Boolean functions $Y = A \oplus B = \bar{A}B + A\bar{B}$ in positive logic.

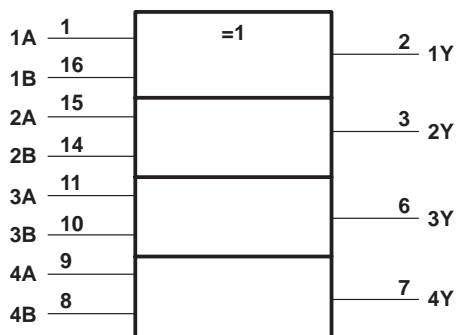
A common application is as a true/complement element. If one of the inputs is low, the other input will be reproduced in true form at the output. If one of the inputs is high, the signal on the other input will be reproduced inverted at the output.

The 74ACT11086 is characterized for operation from -40°C to 85°C .

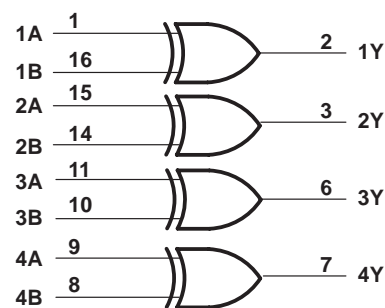
FUNCTION TABLE

| INPUTS | | OUTPUT |
|--------|---|--------|
| A | B | Y |
| L | L | L |
| L | H | H |
| H | L | H |
| H | H | L |

logic symbol†



logic diagram (positive logic)



† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

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exclusive-OR logic

An exclusive-OR gate has many applications, some of which can be represented better by alternative logic symbols.



These are five equivalent exclusive-OR symbols valid for an 'HC86 gate in positive logic; negation may be shown at any two ports.

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

| | |
|--|----------------------------|
| Supply voltage range, V_{CC} | -0.5 V to 7 V |
| Input voltage range, V_I (see Note 1) | -0.5 V to $V_{CC} + 0.5$ V |
| Output voltage range, V_O (see Note 1) | -0.5 V to $V_{CC} + 0.5$ V |
| Input clamp current, I_{IK} ($V_I < 0$ or $V_I > V_{CC}$) | ± 20 mA |
| Output clamp current, I_{OK} ($V_O < 0$ or $V_O > V_{CC}$) | ± 50 mA |
| Continuous output current, I_O ($V_O = 0$ to V_{CC}) | ± 50 mA |
| Continuous current through V_{CC} or GND | ± 100 mA |
| Storage temperature range | -65°C to 150°C |

† Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTE 1: The input and output voltage ratings may be exceeded if the input and output current ratings are observed.

recommended operating conditions

| | | MIN | MAX | UNIT |
|---------------------|------------------------------------|-----|----------|------|
| V_{CC} | Supply voltage | 4.5 | 5.5 | V |
| V_{IH} | High-level input voltage | | 2 | V |
| V_{IL} | Low-level input voltage | | 0.8 | V |
| V_I | Input voltage | 0 | V_{CC} | V |
| V_O | Output voltage | 0 | V_{CC} | V |
| I_{OH} | High-level output current | | -24 | mA |
| I_{OL} | Low-level output current | | 24 | mA |
| $\Delta t/\Delta v$ | Input transition rise or fall rate | 0 | 10 | ns/V |
| T_A | Operating free-air temperature | -40 | 85 | °C |

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

| PARAMETER | TEST CONDITIONS | V _{CC} | T _A = 25°C | | | MIN | MAX | UNIT |
|----------------------------|---|-----------------|-----------------------|-----|------|-------|-----|------|
| | | | MIN | TYP | MAX | | | |
| V _{OH} | I _{OH} = - 50 μA | 4.5 V | 4.4 | | | 4.4 | | V |
| | | 5.5 V | 5.4 | | | 5.4 | | |
| | I _{OH} = - 24 mA | 4.5 V | 3.94 | | | 3.8 | | |
| | | 5.5 V | 4.94 | | | 4.8 | | |
| I _{OH} = - 75 mA† | 5.5 V | | | | 3.85 | | | |
| V _{OL} | I _{OL} = 50 μA | 4.5 V | | | | 0.1 | | V |
| | | 5.5 V | | | | 0.1 | | |
| | I _{OL} = 24 mA | 4.5 V | | | | 0.36 | | |
| | | 5.5 V | | | | 0.36 | | |
| | I _{OL} = 75 mA† | 5.5 V | | | | 1.65 | | |
| I _I | V _I = V _{CC} or GND | 5.5 V | | | | ± 0.1 | | μA |
| I _{CC} | V _I = V _{CC} or GND, I _O = 0 | 5.5 V | | | | 4 | | μA |
| ΔI _{CC} ‡ | One input at 3.4 V, Other inputs at GND or V _{CC} | 5.5 V | | | | 0.9 | | mA |
| C _i | V _I = V _{CC} or GND | 5 V | 3.5 | | | | | pF |

† Not more than one output should be tested at a time, and the duration of the test should not exceed 10 ms.

‡ This is the increase in supply current for each input that is at one of the specified TTL voltage levels rather than 0 V or V_{CC}.

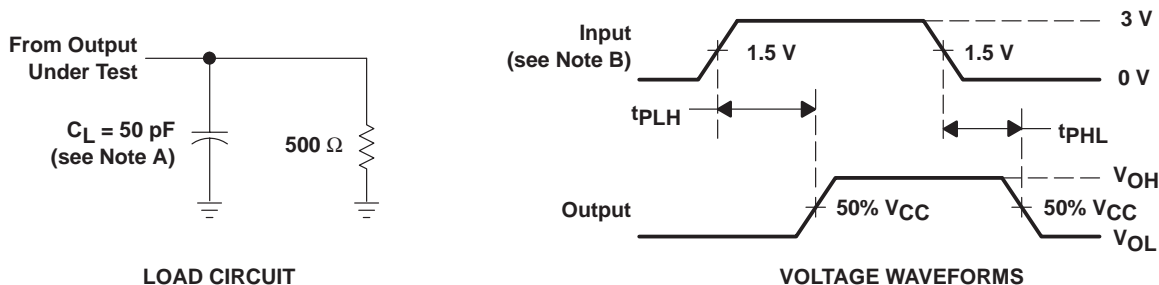
switching characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted) (see Figure 1)

| PARAMETER | FROM (INPUT) | TO (OUTPUT) | T _A = 25°C | | | MIN | MAX | UNIT |
|------------------|--------------|-------------|-----------------------|-----|-----|-----|-----|------|
| | | | MIN | TYP | MAX | | | |
| t _{PLH} | A or B | Y | 1.5 | 5.1 | 8.7 | 1.5 | 9.6 | ns |
| t _{PHL} | | | 1.5 | 5.1 | 8 | 1.5 | 9 | |

operating characteristics, V_{CC} = 5 V, T_A = 25°C

| PARAMETER | TEST CONDITIONS | TYP | UNIT |
|--|-----------------------------------|-----|------|
| C _{pd} Power dissipation capacitance per gate | C _L = 50 pF, f = 1 MHz | 26 | pF |

PARAMETER MEASUREMENT INFORMATION



- NOTES: A. C_L includes probe and jig capacitance.
 B. Input pulses are supplied by generators having the following characteristics: PRR ≤ 10 MHz, Z_O = 50 Ω, t_r = 3 ns, t_f = 3 ns.
 C. The outputs are measured one at a time with one input transition per measurement.

Figure 1. Load Circuit and Voltage Waveforms

PACKAGING INFORMATION

| Orderable Device | Status ⁽¹⁾ | Package Type | Package Drawing | Pins | Package Qty | Eco Plan ⁽²⁾ | Lead/Ball Finish | MSL Peak Temp ⁽³⁾ |
|------------------|-----------------------|--------------|-----------------|------|-------------|-------------------------|------------------|------------------------------|
| 74ACT11086D | OBSOLETE | SOIC | D | 16 | | TBD | Call TI | Call TI |
| 74ACT11086N | OBSOLETE | PDIP | N | 16 | | TBD | Call TI | Call TI |
| 74ACT11086N | OBSOLETE | PDIP | N | 16 | | TBD | Call TI | Call TI |

⁽¹⁾ The marketing status values are defined as follows:

ACTIVE: Product device recommended for new designs.

LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

PREVIEW: Device has been announced but is not in production. Samples may or may not be available.

OBSOLETE: TI has discontinued the production of the device.

⁽²⁾ Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS) or Green (RoHS & no Sb/Br) - please check <http://www.ti.com/productcontent> for the latest availability information and additional product content details.

TBD: The Pb-Free/Green conversion plan has not been defined.

Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.

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⁽³⁾ MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

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