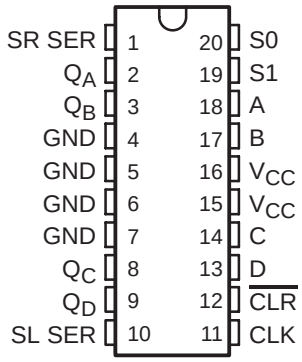
SCAS094 − NOVEMBER 1989 − REVISED APRIL 1993

- **Inputs Are TTL-Voltage Compatible**
- **Parallel-to-Serial, Serial-to-Parallel Conversions**
- **Left or Right Shifts**
- **Parallel Synchronous Loading**
- **Direct Overriding Clear**
- **Temporary Data Latching Capability**
- **Center-Pin V_{CC} and GND Configurations Minimize High-Speed Switching Noise**
- ***EPIC*™ (Enhanced-Performance Implanted CMOS) 1-μm Process**
- **500-mA Typical Latch-Up Immunity at 125°C**
- **Package Options Include Plastic Small-Outline Packages and Standard Plastic 300-mil DIPs**

DW OR N PACKAGE
(TOP VIEW)



description

This bidirectional shift register features parallel outputs, right-shift and left-shift serial inputs, operating-mode-control inputs, and a direct overriding clear line. The register has four distinct modes of operation, namely:

Parallel (broadside) load
Shift right (in the direction Q_A toward Q_D)
Shift left (in the direction Q_D toward Q_A)
Inhibit clocking (do nothing).

Synchronous parallel loading is accomplished by applying the 4 bits of data and taking both mode control inputs, S0 and S1, high. The data are loaded into the associated flip-flops and appear at the outputs after the positive transition of the clock input. During loading, serial data flow is inhibited.

Shift right is accomplished synchronously with the rising edge of the clock pulse when S0 is high and S1 is low. Serial data for this mode is entered at the shift-right data input. When S0 is low and S1 is high, data shifts left synchronously and new data is entered at the shift-left serial inputs. Clocking of the flip-flop is inhibited when both mode control inputs are low.

The 74ACT11194 is characterized for operation from − 40°C to 85°C.

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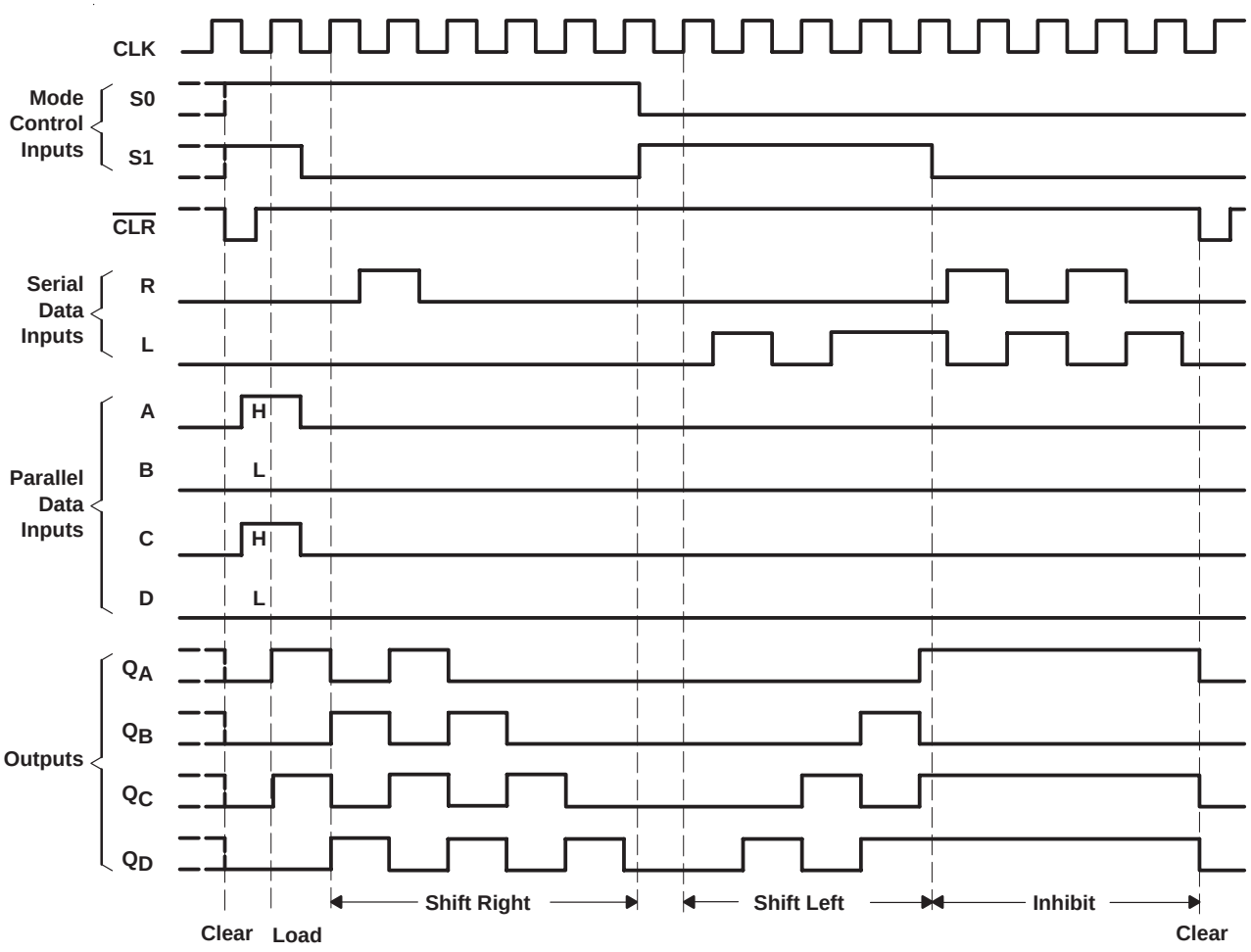
FUNCTION TABLE

INPUTS										OUTPUTS			
$\overline{CLR}$	MODE		CLK	SERIAL		PARALLEL				Q_A	Q_B	Q_C	Q_D
	S1	S0		LEFT	RIGHT	A	B	C	D				
L	X	X	X	X	X	X	X	X	X	L	L	L	L
H	X	X	L	X	X	X	X	X	X	Q_{A0}	Q_{B0}	Q_{C0}	Q_{D0}
H	H	H	↑	X	X	a	b	c	d	a	b	c	d
H	L	H	↑	X	H	X	X	X	X	H	Q_{An}	Q_{Bn}	Q_{Cn}
H	L	H	↑	X	L	X	X	X	X	L	Q_{An}	Q_{Bn}	Q_{Cn}
H	H	L	↑	H	X	X	X	X	X	Q_{Bn}	Q_{Cn}	Q_{Dn}	H
H	H	L	↑	L	X	X	X	X	X	Q_{Bn}	Q_{Cn}	Q_{Dn}	L
H	L	L	X	X	X	X	X	X	X	Q_{A0}	Q_{B0}	Q_{C0}	Q_{D0}

H = high level (steady state)
L = low level (steady state)
X = irrelevant (any input, including transitions)
↑ = transition from low to high level
a,b,c,d = the level of steady-state input at inputs A, B, C, or D, respectively.
Q_{A0}, Q_{B0}, Q_{C0}, Q_{D0} = the level of Q_A, Q_B, Q_C, or Q_D, respectively, before the indicated steady-state input conditions were established.
Q_{An}, Q_{Bn}, Q_{Cn}, Q_{Dn} = the level of Q_A, Q_B, Q_C, or Q_D respectively, before the most-recent ↑ transition of the clock.

timing clear, load, right-shift, inhibit, and clear sequences



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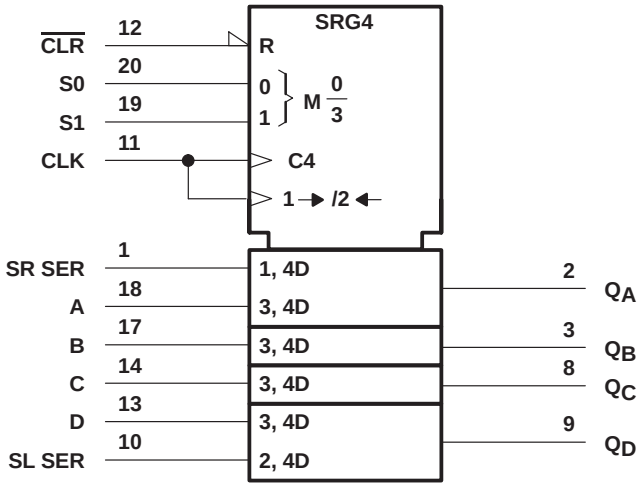
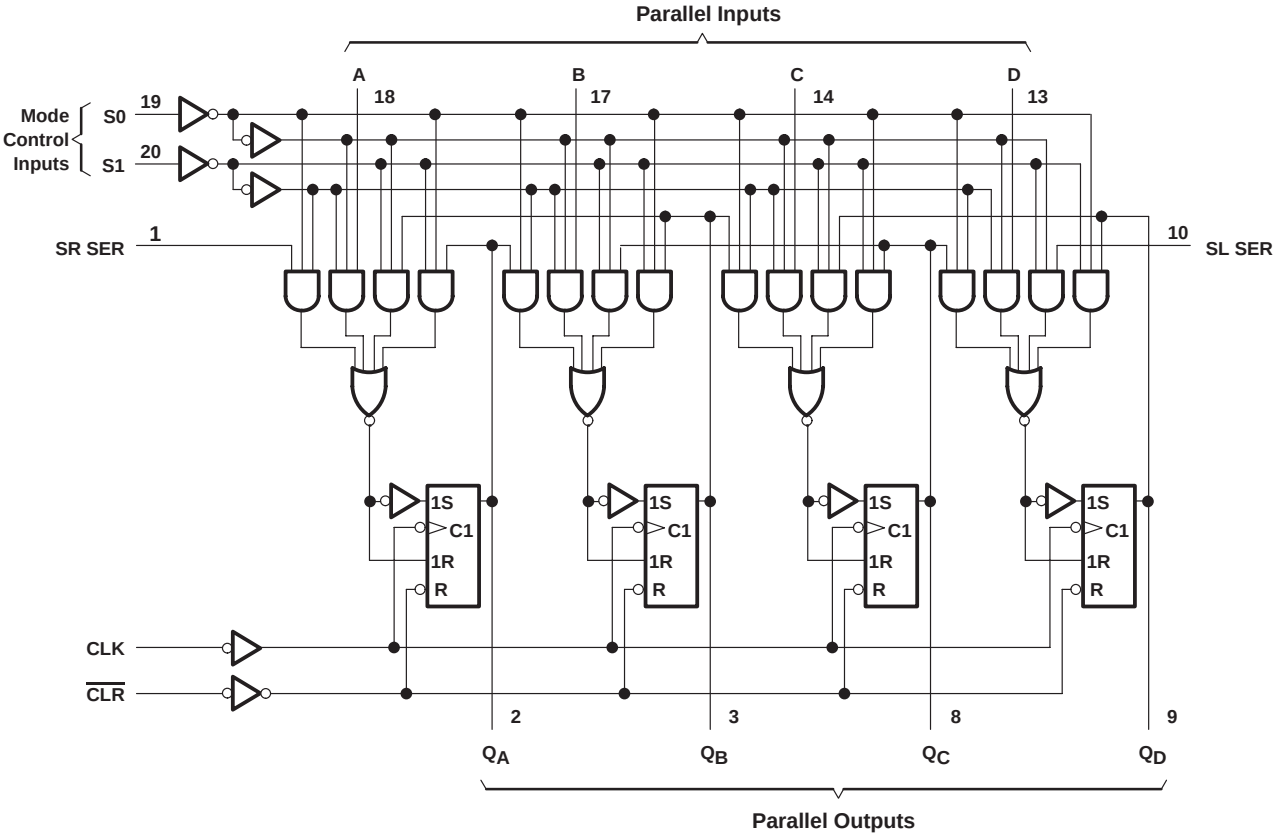
logic symbol†



† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

logic diagram (positive logic)



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage range, V_{CC} . . . . . −0.5 V to 7 V
Input voltage range, V_I (see Note 1) . . . . . −0.5 V to V_{CC} + 0.5 V
Output voltage range, V_O (see Note 1) . . . . . −0.5 V to V_{CC} + 0.5 V
Input clamp current, I_{IK} (V_I < 0 or V_I > V_{CC}) . . . . . ± 20 mA
Output clamp current, I_{OK} (V_O < 0 or V_O > V_{CC}) . . . . . ± 50 mA
Continuous output current, I_O (V_O = 0 to V_{CC}) . . . . . ± 50 mA
Continuous current through V_{CC} or GND . . . . . ± 100 mA
Storage temperature range . . . . . −65°C to 150°C

† Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTE 1: The input and output voltage ratings may be exceeded if the input and output current ratings are observed.

recommended operating conditions

		MIN	NOM	MAX	UNIT
V_{CC}	Supply voltage	4.5		5.5	V
V_{IH}	High-level input voltage	2			V
V_{IL}	Low-level input voltage			0.8	V
V_I	Input voltage	0		V_{CC}	V
V_O	Output voltage	0		V_{CC}	V
I_{OH}	High-level output current			−24	mA
I_{OL}	Low-level output current			24	mA
$\Delta t/\Delta v$	Input transition rise or fall rate	0		10	ns/V
T_A	Operating free-air temperature	− 40		85	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS		V_{CC}	T_A = 25°C			MIN	MAX	UNIT
				MIN	TYP	MAX			
V_{OH}	I_{OH} = − 50 μA		4.5 V	4.4			4.4		V
			5.5 V	5.4			5.4		
	I_{OH} = − 24 mA		4.5 V	3.94			3.8		
			5.5 V	4.94			4.8		
	I_{OH} = − 75 mA‡		5.5 V				3.85		
V_{OL}	I_{OL} = 50 μA		4.5 V			0.1		0.1	V
			5.5 V			0.1		0.1	
	I_{OL} = 24 mA		4.5 V			0.36		0.44	
			5.5 V			0.36		0.44	
	I_{OL} = 75 mA‡		5.5 V					1.65	
I_I	V_I = V_{CC} or GND		5.5 V			± 0.1		± 1	μA
I_{CC}	V_I = V_{CC} or GND,	I_O = 0	5.5 V			8		80	μA
ΔI_{CC}§	One input at 3.4 V,	Other inputs at GND or V_{CC}	5.5 V			0.9		1	mA
C_i	V_I = V_{CC} or GND		5 V		4				pF

‡ Not more than one output should be tested at a time, and the duration of the test should not exceed 10 ms.

§ This is the increase in supply current for each input that is at one of the specified TTL voltage levels rather than 0 V to V_{CC}.

timing requirements over recommended operating free-air temperature range, V_{CC} = 5 V ± 0.5 V (unless otherwise noted) (see Figure 1)

			T_A = 25°C		MIN	MAX	UNIT
			MIN	MAX			
f_{clock}	Clock frequency		0	100	0	100	MHz
t_w	Pulse duration	CLK high or low	5		5		ns
		$\overline{CLR}$ low	4.5		4.5		
t_{su}	Setup time before CLK ↑	Select	6		6		ns
		Data	4		4		
		$\overline{CLR}$ inactive	1		1		
t_h	Hold time after CLK ↑	Select	1.5		1.5		ns
		Data	1		1		

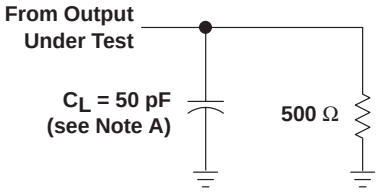
switching characteristics over recommended operating free-air temperature range, V_{CC} = 5 V ± 0.5 V (unless otherwise noted) (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	T_A = 25°C			MIN	MAX	UNIT
			MIN	TYP	MAX			
f_{max}			100	130		100		MHz
t_{PLH}	CLK	Any Q	2.2	5.8	6.9	2.2	7.7	ns
t_{PHL}			2.6	6.6	7.7	2.6	8.8	
t_{PLH}	$\overline{CLR}$	Any Q	2.9	7.1	9.1	2.9	10.3	ns

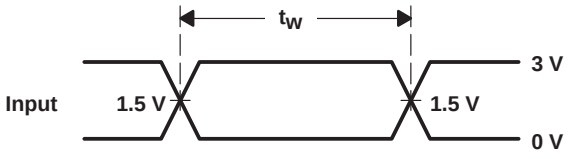
operating characteristics, V_{CC} = 5 V, T_A = 25°C

PARAMETER		TEST CONDITIONS	TYP	UNIT
C_{pd}	Power dissipation capacitance	C_L = 50 pF, f = 1 MHz	69	pF

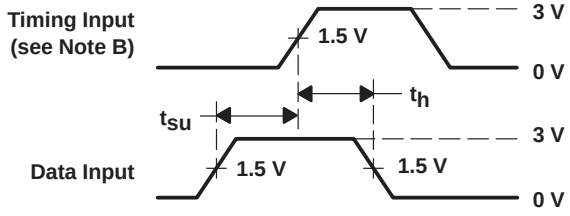
PARAMETER MEASUREMENT INFORMATION



LOAD CIRCUIT



VOLTAGE WAVEFORMS



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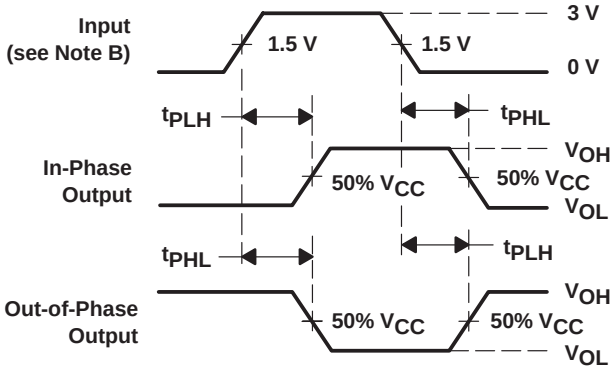

VOLTAGE WAVEFORMS

NOTES: A. C_L includes probe and jig capacitance.
B. All input pulses are supplied by generators having the following characteristics: PRR ≤ 10 MHz, Z_O = 50 Ω, t_r = 3 ns, t_f = 3 ns.
C. The outputs are measured one at a time with one input transition per measurement.

Figure 1. Load Circuit and Voltage Waveforms

PACKAGING INFORMATION

Orderable Device	Status [1]	Package Type	Package Drawing	Pins	Package Qty	Eco Plan [2]	Lead/Ball Finish	MSL Peak Temp [3]
74ACT11194DW	OBSOLETE	SOIC	DW	20		TBD	Call TI	Call TI
74ACT11194N	OBSOLETE	PDIP	N	20		TBD	Call TI	Call TI
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