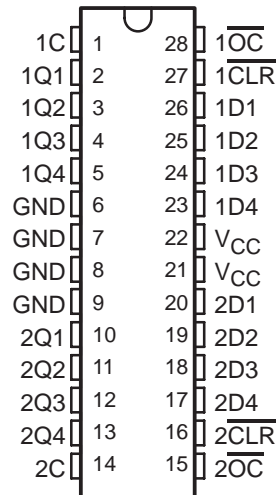


74ACT11873 DUAL 4-BIT D-TYPE LATCH WITH 3-STATE OUTPUTS

SCAS096 – FEBRUARY 1990 – REVISED APRIL 1993

- Inputs Are TTL-Voltage Compatible
- 3-State Buffer-Type Outputs Drive Bus Lines Directly
- Bus-Structured Pinout
- Flow-Through Architecture to Optimize PCB Layout
- Center-Pin V_{CC} and GND Configurations to Minimize High-Speed Switching Noise
- EPIC™ (Enhanced-Performance Implanted CMOS) 1- μ m Process
- 500-mA Typical Latch-Up Immunity at 125°C
- Package Options Include Plastic Small-Outline Packages and Standard Plastic 300-mil DIPs

DW OR NT PACKAGE
(TOP VIEW)



description

These dual 4-bit registers feature 3-state outputs designed specifically for bus driving. This makes these devices particularly suitable for implementing buffer registers, I/O ports, bidirectional bus drivers, and working registers.

The dual 4-bit latch is transparent D-type. When the latch enable input (1C or 2C) is high, the (Q) outputs will follow the data (D) inputs in true form, according to the function table. When the latch enable input is taken low, the outputs will be latched. When \overline{CLR} goes low, the Q outputs go low independently of enable C. The outputs are in a high-impedance state when \overline{OC} (output control) is at a high logic level.

The 74ACT11873 is characterized for operation from -40°C to 85°C .

FUNCTION TABLE

INPUTS				OUTPUT
\overline{OC}	\overline{CLR}	C	D	Q
L	L	X	X	L
L	H	H	H	H
L	H	H	L	L
L	H	L	X	Q_0
H	X	X	X	Z

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PRODUCTION DATA information is current as of publication date. Products conform to specifications per the terms of Texas Instruments standard warranty. Production processing does not necessarily include testing of all parameters.



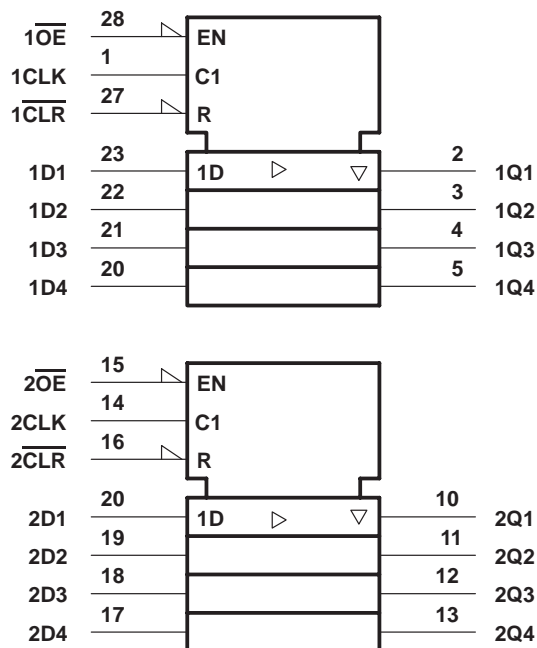
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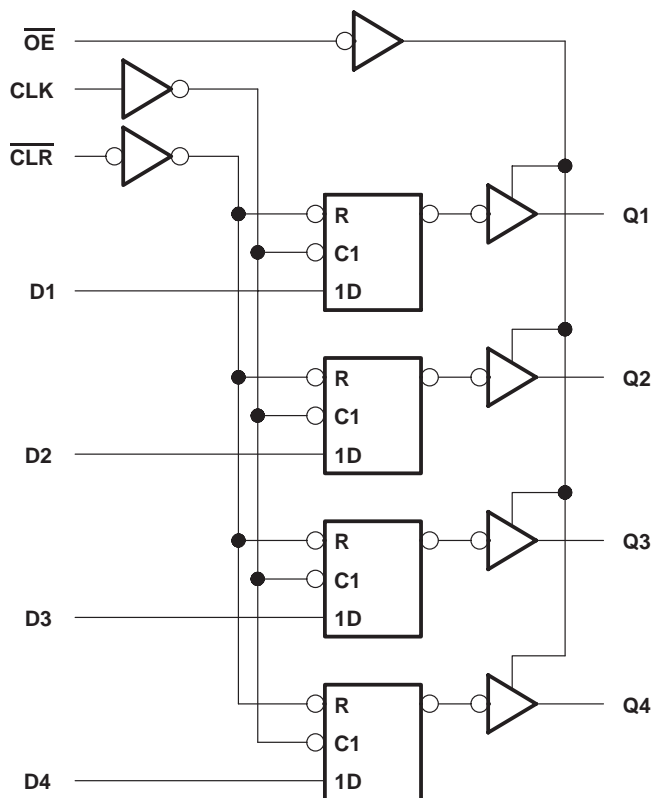
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logic symbol†



† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

logic diagram (positive logic) each quad latch



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)‡

Supply voltage range, V_{CC}	-0.5 V to 7 V
Input voltage range, V_I (see Note 1)	-0.5 V to $V_{CC} + 0.5$ V
Output voltage range, V_O (see Note 1)	-0.5 V to $V_{CC} + 0.5$ V
Input clamp current, I_{IK} ($V_I < 0$ or $V_I > V_{CC}$)	± 20 mA
Output clamp current, I_{OK} ($V_O < 0$ or $V_O > V_{CC}$)	± 50 mA
Continuous output current, I_O ($V_O = 0$ to V_{CC})	± 50 mA
Continuous current through V_{CC} or GND	± 200 mA
Storage temperature range	-65°C to 150°C

‡ Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTE 1: The input and output voltage ratings may be exceeded if the input and output current ratings are observed.

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recommended operating conditions

		MIN	MAX	UNIT
V _{CC}	Supply voltage	4.5	5.5	V
V _{IH}	High-level input voltage	2		V
V _{IL}	Low-level input voltage		0.8	V
V _I	Input voltage	0	V _{CC}	V
V _O	Output voltage	0	V _{CC}	V
I _{OH}	High-level output current		-24	mA
I _{OL}	Low-level output current		24	mA
Δt/Δv	Input transition rise or fall rate	0	10	ns/V
T _A	Operating free-air temperature	-40	85	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS	V _{CC}	T _A = 25°C			MIN	MAX	UNIT
			MIN	TYP	MAX			
V _{OH}	I _{OH} = -50 μA	4.5 V	4.4		4.4		V	
		5.5 V	5.4		5.4			
	I _{OH} = -24 mA	4.5 V	3.94		3.8			
		5.5 V	4.94		4.8			
I _{OH} = -75 mA†	5.5 V			3.85				
V _{OL}	I _{OL} = 50 μA	4.5 V			0.1	0.1	V	
		5.5 V			0.1	0.1		
	I _{OL} = 24 mA	4.5 V			0.36	0.44		
		5.5 V			0.36	0.44		
I _{OL} = 75 mA†	5.5 V				1.65			
I _{OZ}	V _O = V _{CC} or GND	5.5 V			± 0.5	± 5	μA	
I _I	V _I = V _{CC} or GND	5.5 V			± 0.1	± 1	μA	
I _{CC}	V _I = V _{CC} or GND, I _O = 0	5.5 V			8	80	μA	
ΔI _{CC} ‡	One input at 3.4 V, Other inputs at GND or V _{CC}	5.5 V			0.9	1	mA	
C _i	V _I = V _{CC} or GND	5 V		4.5			pF	
C _o	V _O = V _{CC} or GND	5 V		13.5			pF	

† Not more than one output should be tested at a time, and the duration of the test should not exceed 10 ms.

‡ This is the increase in supply current for each input that is at one of the specified TTL voltage levels rather than 0 V to V_{CC}.

timing requirements over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted) (see Figure 1)

		T _A = 25°C		MIN	MAX	UNIT
		MIN	MAX			
t _w	Pulse duration	CLR low	5	5		ns
		C high	5	5		
t _{su}	Setup time before C ↓	Data high	6	6		ns
		Data low	3	3		
t _h	Hold time after C ↓	Data high	0	0		ns
		Data low	0	0		



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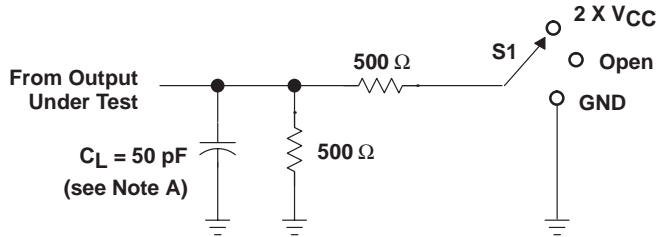
switching characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted) (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	T _A = 25°C			MIN	MAX	UNIT
			MIN	TYP	MAX			
t _{PLH}	D	Q	4.4	7.2	8.8	4.4	10	ns
t _{PHL}			3	6.6	9.1	3	10.2	
t _{PLH}	C	Q	4.7	8.1	10	4.7	11.3	ns
t _{PHL}			5.2	8.9	10.9	5.2	12.3	
t _{PHL}	$\overline{\text{CLR}}$	Q	2.9	6.5	9	2.9	10	ns
t _{PZH}	$\overline{\text{OC}}$	Q	1.9	4.9	7.1	1.9	8	ns
t _{PZL}			2.7	6.4	9.1	2.7	10.3	
t _{PHZ}	$\overline{\text{OC}}$	Q	5.7	8	9.5	5.7	10.2	ns
t _{PLZ}			5.2	7.8	9.1	5.2	9.8	

operating characteristics, V_{CC} = 5 V, T_A = 25°C

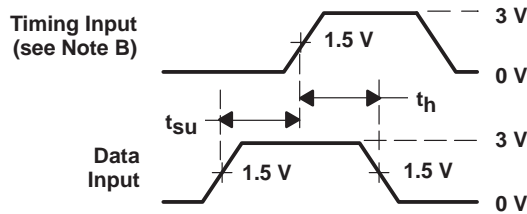
PARAMETER		TEST CONDITIONS	TYP	UNIT
C _{pd}	Power dissipation capacitance per latch	C _L = 50 pF, f = 1 MHz	40	pF
			7	

PARAMETER MEASUREMENT INFORMATION

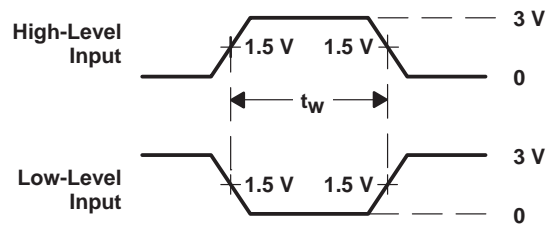


TEST	S1
t_{PLH}/t_{PHL}	Open
t_{PLZ}/t_{PZL}	$2 \times V_{CC}$
t_{PHZ}/t_{PZH}	GND

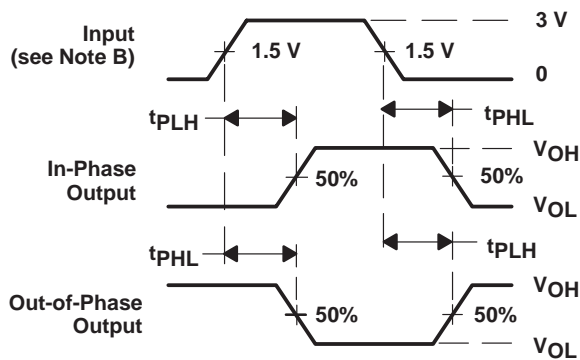
LOAD CIRCUIT



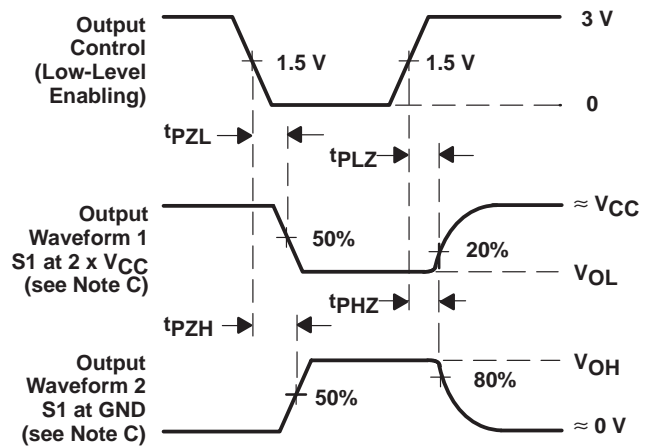
**VOLTAGE WAVEFORMS
 SETUP AND HOLD TIMES**



**VOLTAGE WAVEFORMS
 PULSE DURATION**



**VOLTAGE WAVEFORMS
 PROPAGATION DELAY TIMES**



**VOLTAGE WAVEFORMS
 ENABLE AND DISABLE TIMES**

- NOTES: A. C_L includes probe and jig capacitance.
 B. All input pulses are supplied by generators having the following characteristics: $PRR \leq 10$ MHz, $Z_O = 50 \Omega$, $t_r \leq 2.5$ ns, $t_f \leq 2.5$ ns.
 C. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control.
 Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
 D. The outputs are measured one at a time with one transition per measurement.

Figure 1. Load Circuit and Voltage Waveforms

PACKAGING INFORMATION

Orderable Device	Status ⁽¹⁾	Package Type	Package Drawing	Pins	Package Qty	Eco Plan ⁽²⁾	Lead/Ball Finish	MSL Peak Temp ⁽³⁾
74ACT11873DW	OBSOLETE	SOIC	DW	28		TBD	Call TI	Call TI
74ACT11873NT	OBSOLETE	PDIP	NT	28		TBD	Call TI	Call TI
74ACT11873NT	OBSOLETE	PDIP	NT	28		TBD	Call TI	Call TI

⁽¹⁾ The marketing status values are defined as follows:

ACTIVE: Product device recommended for new designs.

LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

PREVIEW: Device has been announced but is not in production. Samples may or may not be available.

OBSOLETE: TI has discontinued the production of the device.

⁽²⁾ Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS) or Green (RoHS & no Sb/Br) - please check <http://www.ti.com/productcontent> for the latest availability information and additional product content details.

TBD: The Pb-Free/Green conversion plan has not been defined.

Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.

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⁽³⁾ MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

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