- **Members of the Texas Instruments**
  ***Widebus*™ Family**

- **Inputs Are TTL-Voltage Compatible**

- **3-State Inverting Outputs**

- **Flow-Through Architecture Optimizes**
  PCB Layout

- **Distributed V$_{CC}$ and GND Pin Configuration**
  Minimizes High-Speed Switching Noise

- ***EPIC*™ (Enhanced-Performance Implanted**
  CMOS) 1-μm Process

- **500-mA Typical Latch-Up Immunity at**
  125°C

- **Packaged in Plastic 300-mil Shrink**
  Small-Outline (DL) Packages Using 25-mil
  Center-to-Center Pin Spacings and 380-mil
  Fine-Pitch Ceramic Flat (WD) Packages
  Using 25-mil Center-to-Center Pin Spacings

54ACT16475 . . . WD PACKAGE
74ACT16475 . . . DL PACKAGE
(TOP VIEW)

1$\overline{OEAB}$	1	56	1$\overline{OEBA}$
1CLKAB	2	55	1CLKBA
1A1	3	54	1B1
GND	4	53	GND
1A2	5	52	1B2
1A3	6	51	1B3
V$_{CC}$	7	50	V$_{CC}$
1A4	8	49	1B4
1A5	9	48	1B5
1A6	10	47	1B6
GND	11	46	GND
1A7	12	45	1B7
1A8	13	44	1B8
1A9	14	43	1B9
2A1	15	42	2B1
2A2	16	41	2B2
2A3	17	40	2B3
GND	18	39	GND
2A4	19	38	2B4
2A5	20	37	2B5
2A6	21	36	2B6
V$_{CC}$	22	35	V$_{CC}$
2A7	23	34	2B7
2A8	24	33	2B8
GND	25	32	GND
2A9	26	31	2B9
2CLKAB	27	30	2CLKBA
2$\overline{OEAB}$	28	29	2$\overline{OEBA}$
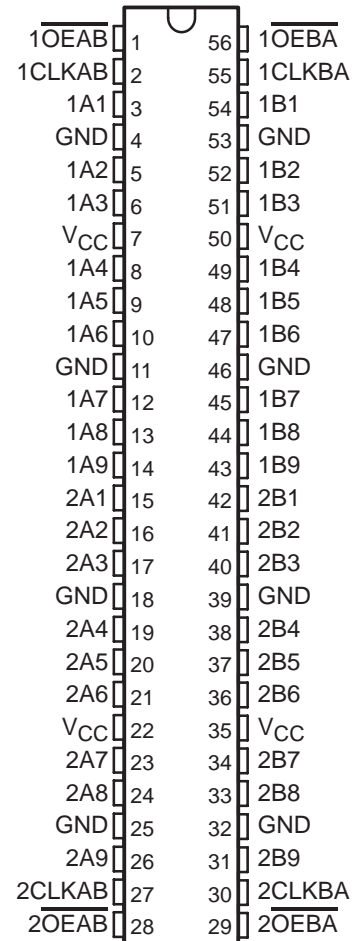
description

The 'ACT16475 are 18-bit registered transceivers that contain two sets of D-type flip-flops for temporary storage of data flowing in either direction. They can be used as two 9-bit transceivers or one 18-bit transceiver. Separate clock (CLKAB and CLKBA) and output-enable ($\overline{OEAB}$ or $\overline{OEBA}$) inputs are provided for each register to permit independent control in either direction of data flow.

Data at the A inputs meeting the setup time requirements is transferred to the B outputs on the positive-going edge of CLKAB. With $\overline{OEAB}$ low, the 3-state B outputs are enabled and reflect the inverted A data. Data flow from B to A is similar but requires the use of the CLKBA and $\overline{OEBA}$ inputs.

The 74ACT16475 is packaged in TI's shrink small-outline package, which provides twice the I/O pin count and functionality of standard small-outline packages in the same printed-circuit-board area.

The 54ACT16475 is characterized for operation over the full military temperature range of –55°C to 125°C. The 74ACT16475 is characterized for operation from –40°C to 85°C.

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TEXAS
INSTRUMENTS

FUNCTION TABLE†

INPUTS			OUTPUT
$\overline{\text{OEAB}}$	CLKAB	A	B
H	X	X	Z
L	L	X	B_0‡
L	↑	L	H
L	↑	H	L

† A-to-B data flow is shown: B-to-A flow is similar but uses CLKBA and $\overline{\text{OEBA}}$.

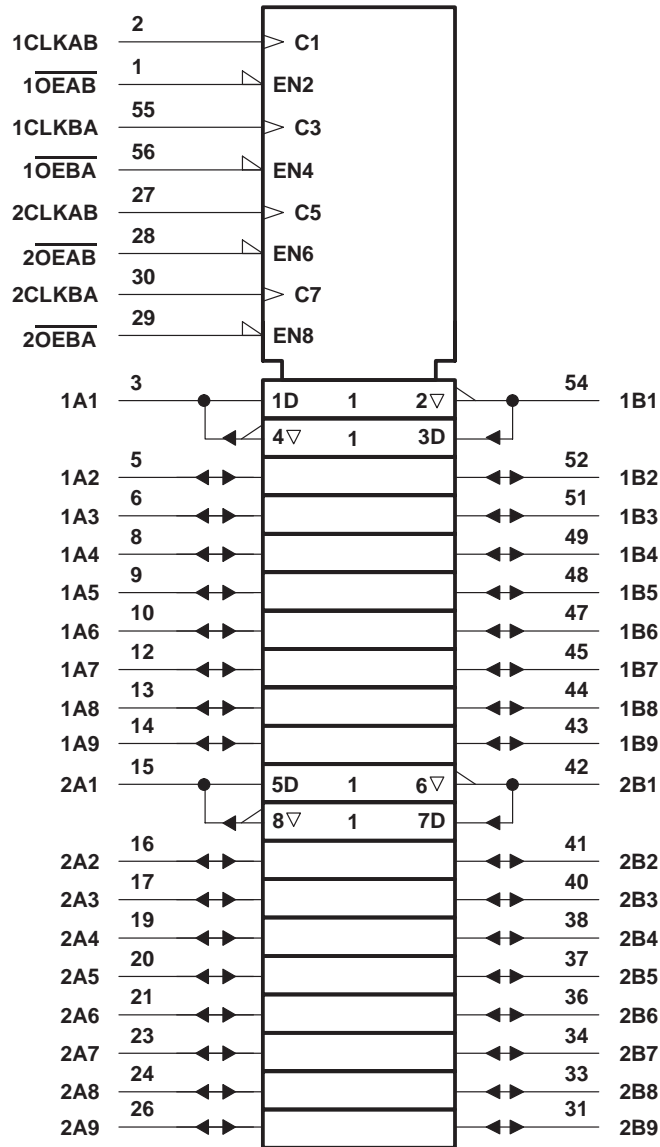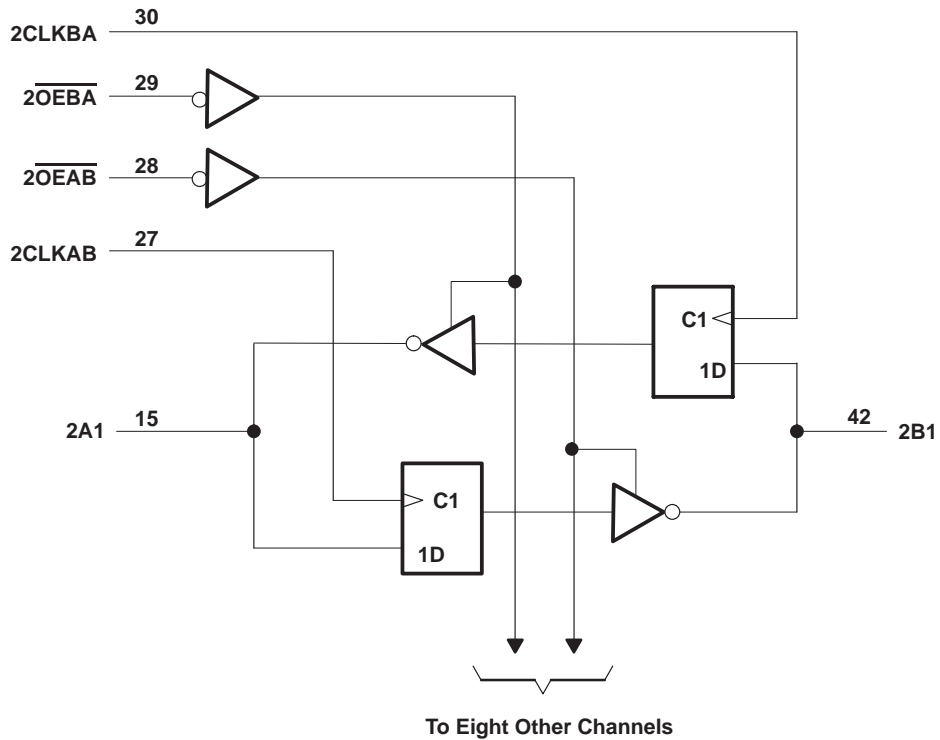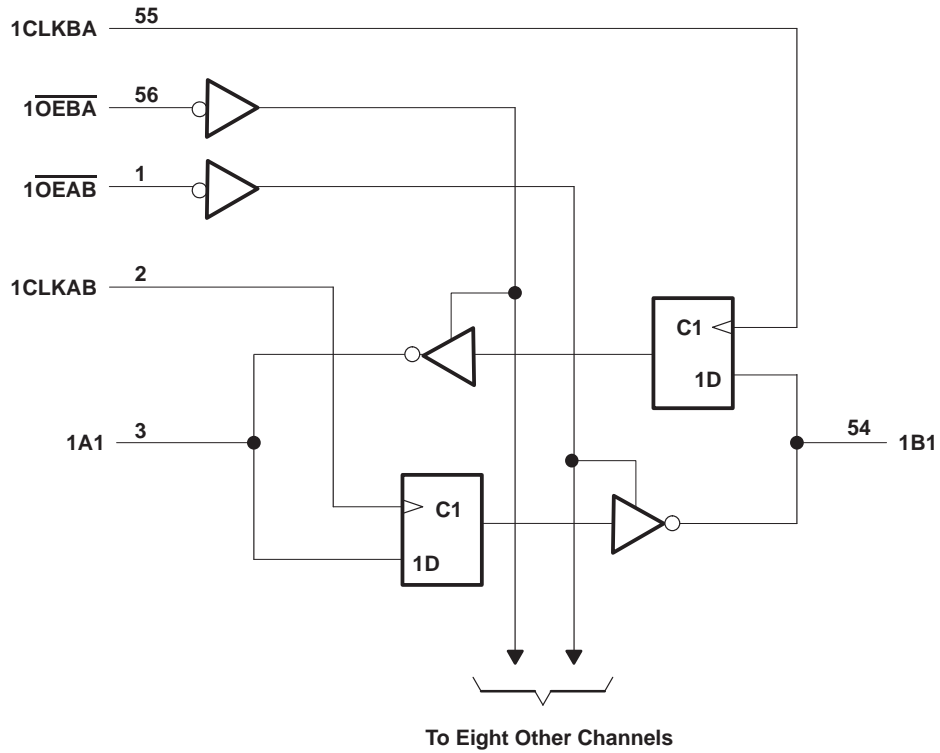‡ Output level before the indicated steady-state input conditions were established

logic symbol§

§ This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

logic diagram (positive logic)

To Eight Other Channels

To Eight Other Channels

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage range, V_{CC} .... −0.5 V to 7 V
Input voltage range, V_I (see Note 1) .... −0.5 V to V_{CC} + 0.5 V
Input voltage range, V_O (see Note 1) .... −0.5 V to V_{CC} + 0.5 V
Input clamp current, I_{IK} (V_I < 0 or V_I > V_{CC}) .... ±20 mA
Output clamp current, I_{OK} (V_O < 0 or V_O > V_{CC}) .... ±50 mA
Continuous output current, I_O (V_O = 0 to V_{CC}) .... ±50 mA
Continuous current through V_{CC} or GND .... ±450 mA
Maximum power package dissipation at T_A = 55°C (in still air) (see Note 2): DL package .... 1.4 W
Storage temperature range, T_{stg} .... −65°C to 150°C

† Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and
  functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not
  implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
NOTES: 1.   The input and output voltage ratings may be exceeded if the input and output current ratings are observed.
            2.   The maximum package power dissipation is calculated using a junction temperature of 150°C and a board trace length of 750 mils.

recommended operating conditions (see Note 2)

		54ACT16475			74ACT16475			UNIT
		MIN	NOM	MAX	MIN	NOM	MAX	
V_{CC}	Supply voltage	4.5	5	5.5	4.5	5	5.5	V
V_{IH}	High-level input voltage	2			2			V
V_{IL}	Low-level input voltage			0.8			0.8	V
V_I	Input voltage	0		V_{CC}	0		V_{CC}	V
V_O	Output voltage	0		V_{CC}	0		V_{CC}	V
I_{OH}	High-level output current			−24			−24	mA
I_{OL}	Low-level output current			24			24	mA
Δt/Δv	Input transition rise or fall rate	0		10	0		10	ns/V
T_A	Operating free-air temperature	−55		125	−40		85	°C

NOTE 3:   Unused pins (input or I/O) must be held high or low to prevent them from floating.

![Texas Instruments logo] **TEXAS INSTRUMENTS**

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	V_{CC}	T_A = 25°C			54ACT16475		74ACT16475		UNIT
				MIN	TYP	MAX	MIN	MAX	MIN	MAX	
V_{OH}		$I_{OH} = -50\ \mu A$	4.5 V	4.4			4.4		4.4		V
			5.5 V	5.4			5.4		5.4		
		$I_{OH} = -24\ mA$	4.5 V	3.94			3.8		3.8		
			5.5 V	4.94			4.8		4.8		
		$I_{OH} = -75\ mA$†	5.5 V				3.85		3.85		
V_{OL}		$I_{OL} = 50\ \mu A$	4.5 V			0.1		0.1		0.1	V
			5.5 V			0.1		0.1		0.1	
		$I_{OL} = 24\ mA$	4.5 V			0.36		0.44		0.44	
			5.5 V			0.36		0.44		0.44	
		$I_{OL} = 75\ mA$†	5.5 V					1.65		1.65	
I_I	Control inputs	$V_I = V_{CC}$ or GND	5.5 V			±0.1		±1		±1	μA
I_{OZ}‡	A or B ports	$V_O = V_{CC}$ or GND	5.5 V			±0.5		±5		±5	μA
I_{CC}		$V_I = V_{CC}$ or GND, I_O = 0	5.5 V			8		80		80	μA
ΔI_{CC}§		One input at 3.4 V, Other inputs at V_{CC} or GND	5.5 V			0.9		1		1	mA
C_i	Control inputs	$V_I = V_{CC}$ or GND	5 V		4.5						pF
C_{io}	A or B ports	$V_O = V_{CC}$ or GND	5 V		12						pF

† Not more than one output should be tested at a time, and the duration of the test should not exceed 10 ms.
‡ For I/O ports, the parameter I_{OZ} includes the input leakage current.
§ This is the increase in supply current for each input that is at one of the specified TTL voltage levels rather than 0 V or V_{CC}.

timing requirements over recommended operating free-air temperature range, V_{CC} = 5 V ± 0.5 V (unless otherwise noted) (see Figure 1)

			T_A = 25°C		54ACT16475		74ACT16475		UNIT
			MIN	MAX	MIN	MAX	MIN	MAX	
f_{clock}	Clock frequency		0	75	0	75	0	75	MHz
t_w	Pulse duration	CLK high or low	6.5		6.5		6.5		ns
t_{su}	Setup time	Data before CLK↑	5.5		5.5		5.5		ns
t_h	Hold time	Data after CLK↑	1.5		1.5		1.5		ns

switching characteristics over recommended operating free-air temperature range, V_{CC} = 5 V ± 0.5 V (unless otherwise noted) (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	T_A = 25°C			54ACT16475		74ACT16475		UNIT
			MIN	TYP	MAX	MIN	MAX	MIN	MAX	
f_{max}			75			75		75		MHz
t_{PLH}	CLKAB or CLKBA	B or A	3.8	7.9	11.1	3.8	12.5	3.8	12.5	ns
t_{PHL}			4.2	8.1	11.4	4.2	12.6	4.2	12.6	
t_{PZH}	$\overline{OEAB}$ or $\overline{OEBA}$	B or A	2.8	7.3	11.4	2.8	12.8	2.8	12.8	ns
t_{PZL}			3.4	7.4	13.1	3.4	14.8	3.4	14.8	
t_{PHZ}	$\overline{OEAB}$ or $\overline{OEBA}$	B or A	5.2	6.5	9.8	5.2	10.5	5.2	10.5	ns
t_{PLZ}			4.5	6.6	9.1	4.5	9.8	4.5	9.8	

![Texas Instruments logo]

operating characteristics, V_{CC} = 5 V, T_A = 25°C

PARAMETER		TEST CONDITIONS		TYP	UNIT
C_{pd} Power dissipation capacitance per transceiver	Outputs enabled	C_L = 50 pF,	f = 1 MHz	27	pF
	Outputs disabled			9	

PARAMETER MEASUREMENT INFORMATION
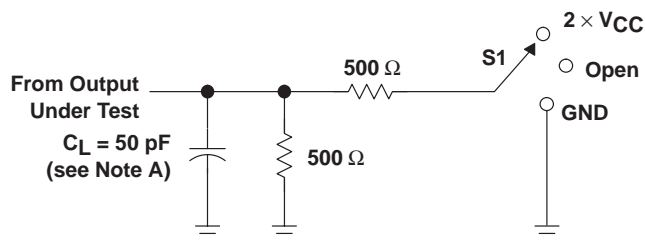
TEST	S1
t_{PLH}/t_{PHL}	Open
t_{PLZ}/t_{PZL}	$2 \times V_{CC}$
t_{PHZ}/t_{PZH}	GND

LOAD CIRCUIT
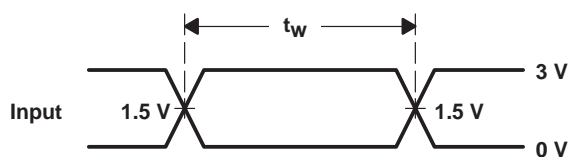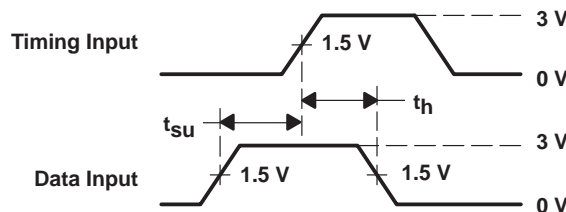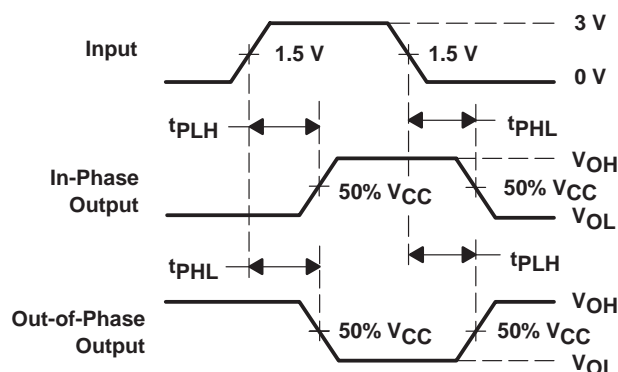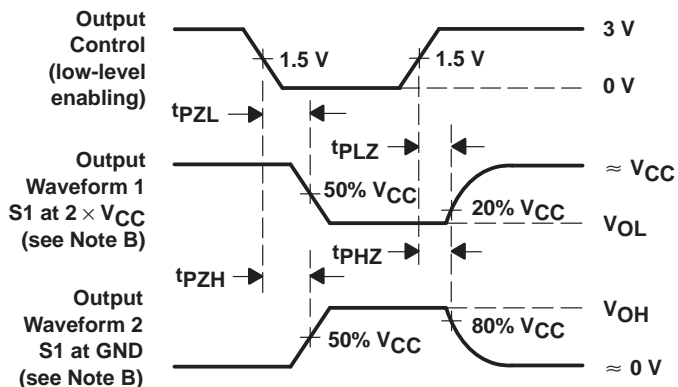
VOLTAGE WAVEFORMS

NOTES: A. C_L includes probe and jig capacitance.
       B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control.
           Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
       C. All input pulses are supplied by generators having the following characteristics: PRR ≤ 1 MHz, Z_O = 50 Ω, t_r = 3 ns, t_f = 3 ns.
       D. The outputs are measured one at a time with one input transition per measurement.

Figure 1. Load Circuit and Voltage Waveforms

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