## 74LVX3L383

10-Bit Low Power Bus-Exchange Switch

## General Description

The LVX3L383 provides two sets of high-speed CMOS TTLcompatible bus switches. The low on resistance of the switch allows inputs to be connected to outputs without adding propagation delay or generating additional ground bounce noise. The device operates as a 10-bit bus switch or a 5 -bit bus exchanger. The bus exchange (BX) signal provides nibble swapping of the $A B$ and $C D$ pairs of signals. This exchange configuration allows byte swapping of buses in systems. It can also be used as a quad 2-to-1 multiplexer and to create low delay barrel shifters. The bus enable (BE) signal turns the switches on.

## Features

- $5 \Omega$ switch connection between two ports
- Zero propagation delay
- Ultra low power with $0.2 \mu$ A typical ICC
- Zero ground bounce in flow-through mode
- Control inputs compatible with TTL level
- Available in SOIC and QSOP (SSOP, $0.15^{\prime \prime}$ body width) packages


## Ordering Code: See Section 11

## Logic Diagram



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## Truth Table

| $\overline{B E}$ | $\mathbf{B X}$ | $\mathbf{A}_{0}-\mathbf{A}_{\mathbf{4}}$ | $\mathbf{B}_{\mathbf{0}}-\mathbf{B}_{\mathbf{4}}$ | Function |
| :---: | :---: | :--- | :--- | :--- |
| $H$ | $X$ | High-Z State | High-Z State | Disconnect |
| L | L | $\mathrm{C}_{0}-\mathrm{C}_{4}$ | $\mathrm{D}_{0}-\mathrm{D}_{4}$ | Connect |
| L | H | $\mathrm{D}_{0}-\mathrm{D}_{4}$ | $\mathrm{C}_{0}-\mathrm{C}_{4}$ | Exchange |

Connection Diagram
Pin Assignment for SOIC and QSOP


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| Pin Names | Description |
| :--- | :--- |
| $\overline{B E}$ | Bus Switch Enable |
| $B X$ | Bus Exchange |
| $A_{0}-A_{4}, B_{0}-B_{4}$ | Buses $A, B$ |
| $C_{0}-C_{4}, D_{0}-D_{4}$ | Buses $C, D$ |


|  | SOIC JEDEC | SSOP JEDEC |
| :--- | :---: | :---: |
| Order Number | 74LVX3L383WM <br> 74LVX3L383WMX | 74LVX3L383QSC <br> 74LVX3L383QSCX |
| See NS <br> Package Number | M24B | MQA24 |

Preliminary Data: National Semiconductor reserves the right to make changes at any time without notice.

Absolute Maximum Ratings (Note 1)
If Military/Aerospace specified devices are required,
please contact the National Semiconductor Sales
Office/Distributors for availability and specifications.
Supply Voltage (VCC)
DC Switch Voltage (VS)
DC Input Voltage (V) (Note 2)
DC Input Diode Current (IIN) with $V_{1}<0$
DC Output (lo) Sink Current
Storage Temperature Range (TSTG)
Power Dissipation
Note 1: The "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. The device should not be operated at these limits. The parametric values defined in the "Electrical Characteristics" table are not guaranteed at the absolute maximum ratings. The "Recommended Operating Conditions" table will define the conditions for actual device operation.
Note 2: The input and output negative voltage ratings may be exceeded if the input and output diode current ratings are observed.

Recommended Operating Conditions
Supply Voltage (VCC) $\quad 4.0 \mathrm{~V}$ to 5.5 V
Free Air Operating Temperature $\left(T_{A}\right) \quad-40^{\circ} \mathrm{C}$ to $+85^{\circ} \mathrm{C}$

## DC Electrical Characteristics

| Symbol | Parameter | $V_{C C}$ <br> (V) |  | 4LVX3L3 |  | Units | Conditions |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: |
|  |  |  | $\mathrm{T}_{\mathrm{A}}=-40^{\circ} \mathrm{C}$ to $+85^{\circ} \mathrm{C}$ |  |  |  |  |
|  |  |  | Min | Typ (Note 3) | Max |  |  |
| $V_{\text {IK }}$ | Maximum Clamp Diode Voltage | 4.5 |  |  | -1.2 | V | $\mathrm{I}_{\mathrm{N}}=-18 \mathrm{~mA}$ |
| $\mathrm{V}_{\mathrm{IH}}$ | Minimum High Level Input Voltage | 4.0-5.5 | 2.0 |  |  | V |  |
| $V_{\text {IL }}$ | Maximum Low Level Input Voltage | 4.0-5.5 |  |  | 0.8 |  |  |
| IN | Maximum Input Leakage Current | 0 |  |  | 10 | $\mu \mathrm{A}$ | $0 \leq \mathrm{V}_{\mathrm{IN}} \leq 5.5 \mathrm{~V}$ |
|  |  | 5.5 |  |  | $\pm 1$ |  |  |
| loz | Maximum TRI-STATE® I/O Leakage | 5.5 |  |  | $\pm 1$ | $\mu \mathrm{A}$ | $0 \leq A, B \leq V_{C C}$ |
| los | Short Circuit Current | 4.5 | 100 |  |  | mA | $\begin{aligned} & V_{1}(A), V_{1}(B)=0 \mathrm{~V} \\ & V_{1}(B), V_{1}(A)=4.5 \mathrm{~V} \end{aligned}$ |
| $\mathrm{R}_{\text {ON }}$ | Switch On <br> Resistance (Note 1) | 4.5 |  | 5 | 7 | $\Omega$ | $\mathrm{V}_{1}=0 \mathrm{~V}, \mathrm{l}_{\mathrm{ON}}=30 \mathrm{~mA}$ |
|  |  |  |  | 10 | 15 | $\Omega$ | $\mathrm{V}_{1}=2.4 \mathrm{~V}, \mathrm{I}_{\mathrm{ON}}=15 \mathrm{~mA}$ |
| ICC | Maximum Quiescent Supply Current | 5.5 |  | 0.2 | 3.0 | $\mu \mathrm{A}$ | $\begin{aligned} & \mathrm{V}_{1}=\mathrm{V}_{\mathrm{CC}}, \mathrm{GND} \\ & \mathrm{l}_{0}=0 \end{aligned}$ |
| $\Delta \mathrm{CCC}$ | Increase in ICC per Input (Note 2) | 5.5 |  |  | 2.5 | mA | $\mathrm{V}_{\mathrm{IN}}=3.4 \mathrm{~V}, \mathrm{I}_{\mathrm{O}}=0$ <br> Per Control Input |

Note 1: Measured by voltage drop between $A$ and $B$ pin at indicated current through the switch. On resistance is determined by the lower of the voltages on the two ( A or B ) pins.
Note 2: Per TTL driven input ( $\mathrm{V}_{\mathbb{N}}=3.4 \mathrm{~V}$, control inputs only). A and B pins do not contribute to ICC .
Note 3: All typical values are at $\mathrm{V}_{\mathrm{CC}}=5.0 \mathrm{~V}, \mathrm{~T}_{\mathrm{A}}=25^{\circ} \mathrm{C}$.

AC Electrical Characteristics: See Section 2 for Test Methodology

| Symbol | Parameter | $V_{C C}$ <br> (V) | 74LVX3L383 |  |  | Units |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: |
|  |  |  | $\begin{gathered} T_{A}=-40^{\circ} \mathrm{C} \text { to }+85^{\circ} \mathrm{C} \\ \mathrm{C}_{\mathrm{L}}=50 \mathrm{pF} \end{gathered}$ |  |  |  |
|  |  |  | Min | $\begin{gathered} \text { Typ } \\ \text { (Note 2) } \end{gathered}$ | Max |  |
| $\begin{aligned} & \mathrm{t}_{\mathrm{PLH}} \\ & \mathrm{t}_{\mathrm{PHL}} \\ & \hline \end{aligned}$ | Data Propagation Delay $A_{n}$ to $B_{n}$ or $B_{n}$ to $A_{n}$ (Note 1) | 4.5 |  |  | 0.25 | ns |
| $t_{P L H}$ $t_{\mathrm{PHL}}$ | Switch Exchange Time $B X$ to $A_{n}$ or $B_{n}$ | 4.5 | 1.5 |  | 6.5 | ns |
| $\begin{aligned} & \mathrm{t}_{\mathrm{PZL}} \\ & \mathrm{t}_{\mathrm{PZH}} \\ & \hline \end{aligned}$ | Switch Enable Time $\overline{B E}$ to $A_{n}, B_{n}$ | 4.5 | 1.5 |  | 6.5 | ns |
| $\begin{aligned} & \mathrm{t}_{\mathrm{PLZ}} \\ & \mathrm{t}_{\mathrm{PHZ}} \end{aligned}$ | Switch Disenable Time $\overline{B E}$ to $A_{n}, B_{n}$ | 4.5 | 1.5 |  | 5.5 | ns |

Note 1: This parameter is guaranteed by design but not tested. The bus switch contributes no propagation delay other than the RC delay of the On resistance of the switch and the load capacitance. The time constant for the switch and alone is of the order of 0.25 ns for 50 pF load. Since this time constant is much smaller than the rise/fall times of typical driving signals, it adds very little propagation delay to the system. Propagation delay of the bus switch when used in a system is determined by the driving circuit on the driving side of the switch and its interaction with the load on the driven side.
Note 2: All typical values are at $\mathrm{V}_{\mathrm{CC}}=5.0 \mathrm{~V}, \mathrm{~T}_{\mathrm{A}}=25^{\circ} \mathrm{C}$.
Capacitance (Note)

| Symbol | Parameter | Typ | Max | Units | Conditions |
| :--- | :---: | :---: | :---: | :---: | :---: |
| $\mathrm{C}_{\mathbb{N}}$ | Control Input Capacitance | 4 |  | pF | $\mathrm{V}_{\mathrm{CC}}=5.0 \mathrm{~V}$ |
| $\mathrm{C}_{I / O}$ (ON) | Input/Output Capacitance | 8 |  | pF | $\mathrm{V}_{\mathrm{CC}}=5.0 \mathrm{~V}$ |
| $\mathrm{C}_{\text {I/O }}$ (OFF) | Input/Output Capacitance | 6 |  | pF | $\mathrm{V}_{\mathrm{CC}}=5.0 \mathrm{~V}$ |

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[^0]:    Note: Capacitance is characterized but not tested.

