80C31BH, 80C51BH, 80C51BHP, 87C51 SPECIFICATION UPDATE

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The 80C31BH, 80C51BH, 80C51BHP, 87C51 may contain design defects or errors known as errata. Characterized errata that may cause the 80C31BH, 80C51BH, 80C51BHP, 87C51's behavior to deviate from published specifications are documented in this specification update.

Copies of documents which have an ordering number and are referenced in this document, or other Intel literature, may be obtained from:

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CONTENTS

REVISION HISTORY

Rev. Date	Version	Description
07/01/96	001	This is the original Specification document. It contains all errata identified to this date.
11/13/96	002	Combined the 87C51 and 8XC51BH Specification Updates. This document covers the 80C31BH, 80C51BH, 80C51BHP, and 87C51. It replaces both 272878-001 and 272884-001. Added specification changes 001, 002, 003. Deleted specification clarification 006. Clarified marking information, erratum 9600001, and specification clarifications 001–005 and 007.
12/11/96	003	Added specification clarification 008.

PREFACE

As of July, 1996, Intel's Semiconductor Products Group has consolidated available historical device and documentation errata into this new document type called the Specification Update. We have endeavored to include all documented errata in the consolidation process, however, we make no representations or warranties concerning the completeness of the Specification Update.

This document is an update to the specifications contained in the Affected Documents/Related Documents table below. This document is a compilation of device and documentation errata, specification clarifications and changes. It is intended for hardware system manufacturers and software developers of applications, operating systems, or tools.

Information types defined in Nomenclature are consolidated into the specification update and are no longer published in other documents.

This document may also contain information that was not previously published.

This document covers the 80C31BH, 80C51BH, 80C51BHP, and 87C51. It replaces both 272878-001 and 272884-001.

Affected Documents/Related Documents

Title	Order
Embedded Microcontrollers	270648-008
MCS® 51 Microcontroller Family User's Manual	272383-002

Nomenclature

Errata are design defects or errors. These may cause the published (component, board, system) behavior to deviate from published specifications. Hardware and software designed to be used with any component, board, and system must consider all errata documented.

Specification Changes are modifications to the current published specifications. These changes will be incorporated in any new release of the specification.

Specification Clarifications describe a specification in greater detail or further highlight a specification's impact to a complex design situation. These clarifications will be incorporated in any new release of the specification.

Documentation Changes include typos, errors, or omissions from the current published specifications. These will be incorporated in any new release of the specification.

NOTE:

Errata remain in the specification update throughout the product's lifecycle, or until a particular stepping is no longer commercially available. Under these circumstances, errata removed from the specification update are archived and available upon request. Specification changes, specification clarifications and documentation changes are removed from the specification update when the appropriate changes are made to the appropriate product specification or user documentation (datasheets, manuals, etc.).

SUMMARY TABLE OF CHANGES

The following table indicates the errata, specification changes, specification clarifications, or documentation changes which apply to the 80C31BH, 80C51BH, 80C51BHP, 87C51 product. Intel may fix some of the errata in a future stepping of the component, and account for the other outstanding issues through documentation or specification changes as noted. This table uses the following notations:

Codes Used in Summary Table

Steps

X:	Errata exists in the stepping indicated. Specification Change or Clarification that applies to this stepping.
(No mark) or (Blank box):	This erratum is fixed in listed stepping or specification change does not apply to listed stepping.

Page

(Page):	Page location of item in this document.

Status

Doc:	Document change or update will be implemented.
Fix:	This erratum is intended to be fixed in a future step of the component.
Fixed:	This erratum has been previously fixed.
NoFix:	There are no plans to fix this erratum.
Eval:	Plans to fix this erratum are under evaluation.

Row

▌	Change bar to left of table row indicates this erratum is either new or modified from the previous version of the document.

Errata

Number	Steppings				Page	Status	ERRATA
	C-0	C-1	D	E			
9600001	X				7	Fixed	Lockup (80C31BH)

Specification Changes

Number	Steppings				Page	Status	SPECIFICATION CHANGES
	C-0	C-1	D	E			
001			X		7	Doc	New Icc Values in Active and Idle Modes (80C31BH, 80C51BH, 80C51BHP, 87C51)
002			X		8	Doc	Lock Bits Moved to UPROM to Enhance Security (87C51)
003			X		9	Doc	External Connection of EA#/Vpp to Vss No Longer Required (80C31BH)

Specification Clarifications

Number	Steppings				Page	Status	SPECIFICATION CLARIFICATIONS
	C-0	C-1	D	E			
001		X			9	Doc	ROM Verify (80C51BH)
002		X			9	Doc	Lih on Ports 1, 2, 3
003		X			9	Doc	Vcc Rise Time and Power-up Without Reset
004		X			10	Doc	ALE Is Not a Synchronization Signal
005		X			10	Doc	Upper 128 Bytes of RAM Not Implemented
007			X		10	Doc	ESD Testing
008	X	X	X		10	Doc	Port 1 and 3 Reset Value

Documentation Changes

Number	Document Revision	Page	Status	DOCUMENTATION CHANGES
				None for this revision of the Specification Update

IDENTIFICATION INFORMATION

Markings

Microcontroller	Stepping	Identifier	Stepping	Identifier
80C31BH	D	See below	E	A
80C51BH	D	See below	E	A
80C51BHP	D	See below		
87C51	D	A	E	A

The markings that identify D-step 80C31BH and 80C51BH microcontrollers differ depending on the manufacturer. Identifiers are included in the FPO number located on the top of the microcontroller, line 3 for QFP packages, line 2 for other packages.

- A 9-character FPO number ending in “2” (for 80C31BH) or “D” (for 80C51BH) identifies a D-step microcontroller manufactured by Intel.
- A 7-character FPO number beginning with “E” and ending in “2” identifies a D-step microcontroller manufactured by Matsushita Electronics Corporation (MEC). “Japan” is also stamped on the top side.
- A 7-character FPO number beginning with “Y” identifies a D-step microcontroller manufactured by Taiwan Semiconductor Manufacturing Corporation (TSMC). “Taiwan” is also stamped on the top side (before WW08, 1989) or bottom side (after WW08, 1989).

Production of D-step 80C31BH and 80C51BH microcontrollers began in Q1 of 1989. Any 80C31BH or 80C51BH manufactured before 1989 is not a D-step microcontroller.

The following changes were made in D-step 80C31BH and 80C51BH microcontrollers.

- Added ONCE mode and ROM Verify mode.
- Fixed power-on reset and high Ipd errata.

ERRATA

9600001. Lockup (80C31BH)

PROBLEM: Occasionally, an 80C31BH (C-0 stepping) locks up on power-up. In this state, ALE and PSEN# are stuck at zero, and the microcontroller does not respond to reset.

IMPLICATION: During power-up, some internal nodes may come up in a certain combination of states that cause the device to lock up completely. This combination of states never occurs while Vcc is up, but can occur during the randomness of powering up.

WORKAROUND: Bringing RESET up simultaneously with Vcc prevents the lockup combination from occurring. To avoid lockup in the 80C31BH (C-0 stepping), application circuits must bring RESET up along with Vcc. Applications that use the standard power-on reset circuit (a capacitor from RESET to Vcc) bring RESET up with Vcc and do not cause lock-up. Applications in which RESET is driven by a gate might not bring RESET up with Vcc, so they may cause lock-up. In such cases, a pullup resistor from RESET to Vcc has provided a fix.

STATUS: Fixed. Refer to Summary Table of Changes for affected steppings.

SPECIFICATION CHANGES

001. New Icc Values in Active and Idle Modes (80C31BH, 80C51BH, 80C51BHP, 87C51)

PROBLEM: The 80C31BH, 80C51BH, 80C51BHP, and 87C51 have new maximum and typical values for Icc in Active and Idle Modes.

IMPLICATION: Your design must take these values into consideration.

Frequency (MHz)	Active Mode		Idle Mode	
	Maximum Icc (mA)	Typical Icc (mA)	Maximum Icc (mA)	Typical Icc (mA)
12	25 (was 20)	14.5 (was11.5)	9.5 (was 7.5)	8 (was 3.5)
16	30 (was 26)	18 (N/A)	11.5 (was 9.5)	9.5 (N/A)
24	40 (was 38)	24.5 (N/A)	15.5 (was 13.5)	11.5 (N/A)
33	45 (N/A)	32.5 (N/A)	17 (N/A)	13.5 (N/A)

002. Lock Bits Moved to UPROM to Enhance Security (87C51)

PROBLEM: To enhance security, the lock bits have been moved from EPROM to UPROM. The UPROM is a secure area on the device; values written to UPROM cannot be changed. The function of the lock bits, the method for programming them, and the use of the encryption array remain unchanged.

IMPLICATION: Verify that your EPROM code is correct before setting any lock bits. Because the lock bits are in UPROM, the lock bits cannot be changed after they are programmed once. If you set only LB1, you can still verify your code, but you cannot reprogram the EPROM (although you can still erase it using ultraviolet light). If you set LB2, you can no longer verify the EPROM code.

Security Level	Lock Bit			Protection Level
	LB3	LB2	LB1	
1	U	U	U	No program lock features are implemented. On-chip code memory verification is enabled. If you have programmed an encryption array, on-chip program code is encrypted before it is placed onto the data bus for verification.
2	U	U	P	Code executing from external memory cannot fetch code bytes from on-chip code memory (MOVC disabled). On-chip code memory verification is enabled. If you have programmed an encryption array, on-chip program code is encrypted before it is placed onto the data bus for verification.
3	U	P	P	Code executing from external memory cannot fetch code bytes from on-chip code memory (MOVC disabled). On-chip code memory verification is disabled.
4	P	P	P	Code cannot execute from external memory. On-chip code memory verification is disabled.

U = unprogrammed; P= programmed. Other combinations of the lock bits are undefined.

003. External Connection of EA#/Vpp to Vss No Longer Required (80C31BH)

PROBLEM: The 80C31BH's EA#/Vpp pin (pin 31 of the 40-pin DIP, pin 35 of the 44-pin PLCC, or pin 29 of the 44-pin QFP) enables external memory access. For C steppings, applications were required to tie EA# to Vss to enable the microcontroller to fetch code from external program memory. For D steppings, the EA# function is internally connected to Vss instead of through an external pin.

IMPLICATION: Applications using the D stepping 80C31BH microcontroller are not required to tie the EA# pin to Vss externally. However, the pin may optionally be tied to Vss to maintain compatibility with existing designs.

SPECIFICATION CLARIFICATIONS

001. ROM Verify (80C51BH)

PROBLEM: The C-1 stepping of the 80C51BH does not support ROM Verify mode. Therefore, the microcontroller will not verify in an EPROM programmer. The ROM can be verified by using MOVC instructions to access code in the 80C51BH. Schematics and code necessary to do a ROM verify in this way are available on request.

002. Lih on Ports 1, 2, 3

PROBLEM: The Lih (logical 1 input current) is not specified for ports 1, 2, and 3. This value is negligible because of the internal pullups on ports 1, 2, and 3. The value can be considered zero for design considerations.

003. Vcc Rise Time and Power-up Without Reset

PROBLEM: Vcc should rise within approximately 10 milliseconds after power-up. If the Vcc rise time is too long, the microcontroller might lock up or enter an undetermined state. In such cases, power down the microcontroller, then power up again with a faster rise time.

Powering up the device without a valid reset might cause the CPU to start executing instructions from an indeterminate location. Without a valid reset, the SFRs (and specifically the program counter) might not be properly initialized.

004. ALE Is Not a Synchronization Signal

PROBLEM: Although ALE can be used as a clock-out signal, varying propagation delays prevent using ALE as a synchronization signal. Propagation delays from internal timing (XTAL) to the external control signals are typically 25ns to 125ns depending on the pin, temperature, pin loading, Vcc, and manufacturing lot. At room temperature and with the load capacitance at the test condition specified in AC Characteristics, typical propagation delays are approximately 50 ns for RD# and WR# and approximately 85ns for other control signals. Timings given in AC Characteristics include the propagation delays.

005. Upper 128 Bytes of RAM Not Implemented

PROBLEM: In MCS 51 microcontrollers that implement 256 bytes of internal RAM, the upper 128 bytes of RAM can be used as stack space. (Stack operations use indirect addressing.)

The 80C31BH, 80C51BH, 80C51BHP, 87C51 implement only 128 bytes of internal RAM. In these microcontrollers, if the stack pointer points to the upper 128 bytes, PUSHed bytes are lost and POPped bytes are indeterminate.

007. ESD Testing

PROBLEM: The electrostatic discharge (ESD) test measures the resistance of all microcontroller pins to static electricity from both human body and charged devices. All ESD testing at Intel is based on MilStd 883-3015 and more rigorous standards.

The 80C31BH, 80C51BH, 80C51BHP, 87C51 meet the following specifications:

- The Military Standard Method for ESD testing, which includes ±2000 volts, 5 pulses, 1500 ohms, 100 pF to each port with respect to Vss.
- The Charge Device ESD test, which requires ±2000 volts, 5 pulses to each port.

008. Port 1 and 3 Reset Value

PROBLEM: The reset value of all ports is logic “1”; however, the reset value of ports 1 and 3 is sustained by a weak pull-up. It is recommended that applications **not** use the reset value of these ports to drive external loads. If the application requires the use of the reset value of these ports, an external pull-up resistor should be added.

DOCUMENTATION CHANGES

None for this revision of this specification update.