Intel® 82093AA I/O Advanced Programmable Interrupt Controller (I/O APIC)

Specification Update

January 2001

Notice: The Intel® 82093AA (I/O APIC) may contain design defects or errors known as errata which may cause the product to deviate from published specifications. Current characterized errata are documented in this Specification Update.

Document Number: 290710-001

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Revision History

Rev.	Draft/Changes	Date
-001	Initial Release	January 2001

Preface

This document is an update to the specifications contained in the documents listed in the following Affected Documents/Related Documents table. It is a compilation of device and document errata and specification clarifications and changes, and is intended for hardware system manufacturers and for software developers of applications, operating system, and tools.

Information types defined in the Nomenclature section of this document are consolidated into this update document and are no longer published in other documents. This document may also contain information that has not been previously published.

Affected Documents/Related Documents

Document Title	Document Number
Intel® 82093AA I/O Advanced Programmable Interrupt Controller (I/O APIC) datasheet	290566-001

Nomenclature

Specification Changes are modifications of the 82093AA IO Advanced Programmable Interrupt Controller (I/O APIC) . These changes will be incorporated in the next release of the specifications.

Errata are design defects or errors. Errata may cause the 82093AA IO Advanced Programmable Interrupt Controller (I/O APIC) behavior to deviate from published specifications. Hardware and software designed to be used with any given stepping must assume that all errata documented for that stepping are present on all devices.

Specification Clarifications describe a specification in greater detail or further highlight a specification's impact to a complex design situation. These clarifications will be incorporated in the next release of the specifications.

Documentation Changes include typos, errors, or omissions from the current published specifications. These changes will be incorporated in the next release of the specifications.

Component Identification via Programming Interface

The 82093AA I/O Advanced Programmable Interrupt Controller (I/O APIC) may be identified by the following register contents:

Component Identification via Programming Interface (PMC Only)

Register	APIC Offset	Value
IOAPICVER	01h	00170011h

Component Marking Information

The Basic Intel 82093AA I/O APIC may be identified by the following component markings:

Product Number	Vendor ID	Device ID	Revision ID	Product Stepping	Frequency	S-Spec	V_{CC}	T_{CASE}	Notes
82093AA	n/a	n/a	N/a	A1	Note 2	U045	5V ± 10%	0°C - 70°C	1,2
82093AA	n/a	n/a	N/a	A1	Note 2	SL3HY	5V ± 10%	0°C - 70°C	1,2

NOTES:
1. The I/O APIC is memory mapped and therefore does not have Vendor, Device, or Revision ID registers at the PCI specification-defined locations.
2. The I/O APIC frequency at the APIC bus can be 16.666MHz

Component Marking Information

The 82093AA IO Advanced Programmable Interrupt Controller (I/O APIC) may be identified by the following component markings:

Stepping	S-Spec	Top Marketing	Notes
A-1	U045	82093AA S U045	Production
A-1	Q786ES	82093AA S Q786ES	Engineering Samples (Fab Conversion, Change Notification #891, LSI (IOAPIC) Fab 1 to Fab 2 Conversion, November 1, 1999)
A-1	SL3HY	82093AA S L3HY	Production

Summary Table of Changes

The following table indicates the Specification Changes, Errata, Specification Clarifications or Documentation Changes which apply to the listed Intel® 82093AA I/O APIC steppings. Intel intends to fix some of the errata in a future stepping of the component and to account for the other outstanding issues through documentation or Specification Changes as noted. This table uses the following notations:

Codes Used in Summary Table

X:	Erratum, Specification Change or Clarification that applies to this stepping.
Doc:	Document change or update that will be implemented.
Fix:	This erratum is intended to be fixed in a future stepping of the component.
Fixed:	This erratum has been previously fixed.
NoFix	There are no plans to fix this erratum.
(No mark) or (Blank Box):	This erratum is fixed in listed stepping or specification change does not apply to listed stepping.
Shaded:	This item is either new or modified from the previous version of the document.

Number	SPECIFICATION CHANGES
	There are no specification changes in this Specification Update revision

NO.	A0	PLANS	430HX	440FX	ERRATA
					There are no errata in this Specification Update revision

NO.	SPECIFICATION CLARIFICATIONS
1	I/O APIC Pin Description for APICACK2#

Number	DOCUMENTATION CHANGES
	There are no documentation changes in this Specification Update revision

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Specification Changes

There are no specification changes in this Specification Update revision.

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Errata

There are no errata in this Specification Update revision.

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Specification Clarifications

1. I/O APIC Pin Description for APICACK2#

Reference the *82093AA I/O Advanced Programmable Interrupt Controller (I/O APIC)* datasheet, page 6.

Add a new sentence to the existing pin description for APICACK2# so that the description reads:

"**APIC ACKNOWLEDGE 2**: This signal is the second half of the acknowledge handshake indicating that the APIC can send the interrupt message over the APIC bus. This signal is typically connected to the host-to-PCI bridge and along with APICREQ# and APICACK1# makes up the complete buffer coherency protocol cycles. As a result, the I/O APIC ignores all transitions on the APICACK2# signal unless APICACK1# detection has occurred. If the system does not have a host-to-PCI bridge, this signal can be tied low."

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Documentation Changes

There are no documentation changes in this Specification Update revision.