DESCRIPTION

The 8225 is a TTL 64-bit Read-Write Random Access Memory organized as 16-words of 4 bits each. The 8225 is ideally suited for application in scratch pads and high-speed buffer memories.

Words are selected through a 4-input binary decoder when the chip enable input ($\overline{CE}$) is at logic "0". Data is written into the memory when Read Enable (RE) is at logic "0" and read from the memory when RE is at logic "1".

The outputs of the 8225 are logical "1" during write operation, therefore, inputs and outputs can be commoned in busses to reduce the number of I/O leads. Output collectors are uncommitted.

FEATURES

- CHIP ENABLE LINE FOR EXPANSION
- OPEN COLLECTOR OUTPUTS FOR EXPANSION
- ON THE CHIP DECODING
- ALL OUTPUTS "1" DURING WRITING
- DIODE PROTECTED INPUTS

APPLICATIONS

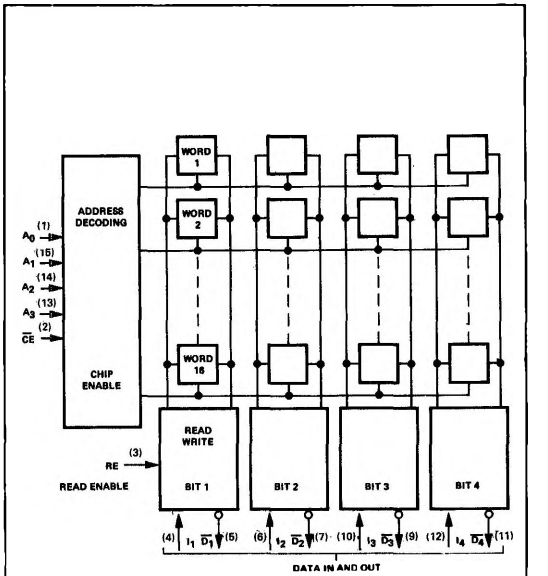
SCRATCH PAD MEMORY
BUFFER MEMORY
PUSH DOWN STACKS (First in-first out)
CONTROL STORE

TRUTH TABLE

RE	$\overline{CE}$ (Chip Enable)	MODE	OUTPUTS
0	0	Write	"1"
1	0	Read	Information
X	1	Chip Disable	"1"

X = Either State

BLOCK DIAGRAM



V_{CC} = (16)
GND = (8)
( ) = Denotes Pin Numbers

"ONE" LEVEL IN OR DATA INPUT APPEARS AS "ZERO" LEVEL OUT.

Chip is enabled when $\overline{CE}$ = "0"

ELECTRICAL CHARACTERISTICS ($0°C \leq T_A$ 75°C ; $4.75V \leq V_{CC} \leq 5.25V$)

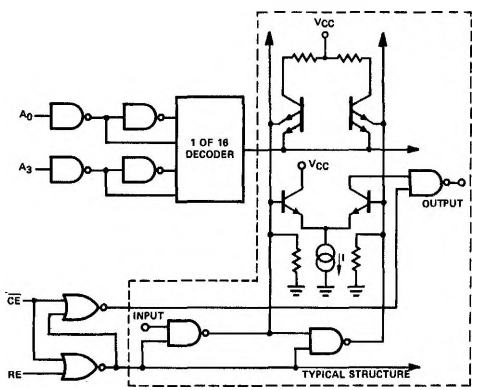
CHARACTERISTICS	LIMITS				CHIP ENABLE	INPUTS		DATA INPUTS	OUTPUTS	NOTES
	MIN.	TYP.	MAX.	UNITS		WRITE	ADDRESS			
"0" Output Voltage			.4	V	.8V	Pulse			16mA	8, 11, 12
"1" Output Leakage Current			100	μA	.8V	Pulse		.8V	5.25V	11, 12
"0" Input Current	-.1		-1.6	mA	.4V	.4V	.4V	.4V		16
"1" Input Current										
Chip Enable			80	μA	4.5V					
Write, Address, Data			40	μA	4.5V	4.5V	4.5V	4.5V		16

T_A = 25°C and V_{CC} = 5.0V

CHARACTERISTICS	LIMITS				CHIP ENABLE	INPUTS		DATA INPUTS	OUTPUTS	NOTES
	MIN.	TYP.	MAX.	UNITS		WRITE	ADDRESS			
Minimum Write Pulse Width (W_{PW})		18	30	ns						
Input Setup Time (I_{SU})		18	20	ns						
Input Hold Time (I_{HO})		0	5	ns						
Address Setup Time (A_{SU})			5	ns						
Address Hold Time (A_{HO})			5	ns						
Access Time (T_A)	20	35	50	ns						17
Data Pulse Width (D_{PW})	20			ns						
Write Recovery Time (T_{WR})	10	25	40	ns						
Write Access Time (T_{WA})		25	40	ns						
Chip Enable Recovery Time (T_{CR})		20	30	ns						
Chip Enable Access Time (T_{CA})		20	30	ns						
Input Clamp Voltage			-1.5	V	-12mA	-12mA	-12mA	-12mA		16
Input Latch Voltage - except Data			5.5	V	10mA	10mA	10mA			16
Data			5.5	V	5V	5V		10mA		16
Power Consumption		400	552	mW	0V	5V	0V	0V		14

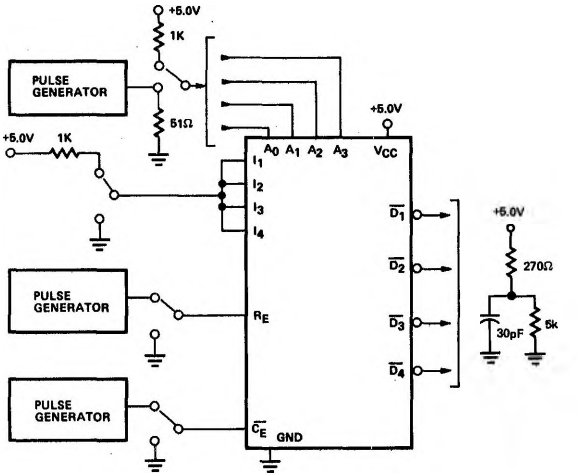
NOTES:
1. All voltage measurements are referenced to the ground terminal. Terminals not specifically referenced are left electrically open.
2. All measurements are taken with ground pin tied to zero volts.
3. Positive current is defined as into the terminal referenced.
4. Positive logic definition: "UP" Level = "1", "DOWN" Level = "0".
5. Precautionary measures should be taken to ensure current limiting in accordance with Absolute Maximum Ratings should the isolation diodes become forward biased.
6. Capacitance is measured on Boonton Electronic Corporation Model 75A-53 Capacitance Bridge or equivalent. f = 1 MHz, V_{ac} = 25m V_{rms}.
7. All pins not specifically referenced are tied to ground for capacitance tests. Output pins are left open.
8. Output sink current is supplied through a resistor to V_{CC}.
9. One DC fan-out is defined as 0.8mA.
10. Manufacturer reserves the right to make design and process changes and improvements.
11. By DC tests per the truth table, all inputs have guaranteed thresholds of 0.8V for logical "0" and 2.0V for logical "1".
12. For any given binary code on the Address Inputs the Write input must be momentarily brought to a logical "0" level.
13. See AC test circuits on following pages.
14. All sense outputs in "0" state.
15. This test guarantees operation free of input latch-up over the specified operating power supply voltage range.
16. Test each input one at a time.
17. Address Pulse Width (A_{PW}) is 40ns for this test.

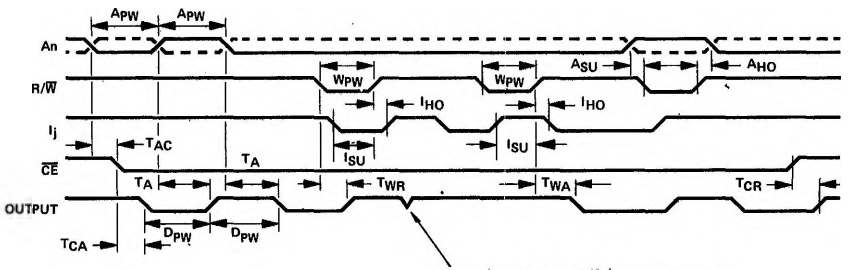
FUNCTIONAL DIAGRAM



ONE LEVEL IN ON DATA INPUT APPEARS AS "ZERO" LEVEL OUT.

AC TEST FIGURES AND WAVEFORMS





NOTE: NEGATIVE TRANSITION DOES NOT GO BELOW 2.6 VOLTS AND GENERALLY IS NOT MEASURABLE.