8228-F

DESCRIPTION

The 8228, available in a 16-pin dual-in-line package, can provide very high bit packing density by replacing 4 standard 256X4 ROMs.

This device includes on-chip decoding, and has a typical access time of 50ns with a power consumption of only .125mW per bit.

The standard 8228 ROM pattern is the USASCII Row Character Generator code; however, custom patterns are also available. The standard pattern is specified as the N8228I-CB162, while custom circuits are identified as N8228I-CXXX.

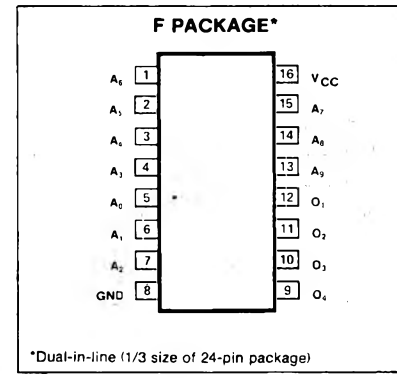
FEATURES

- **Buffered address lines**
- **Totem pole outputs**
- **Diode protected inputs**
- **Fully TTL compatible**

APPLICATIONS

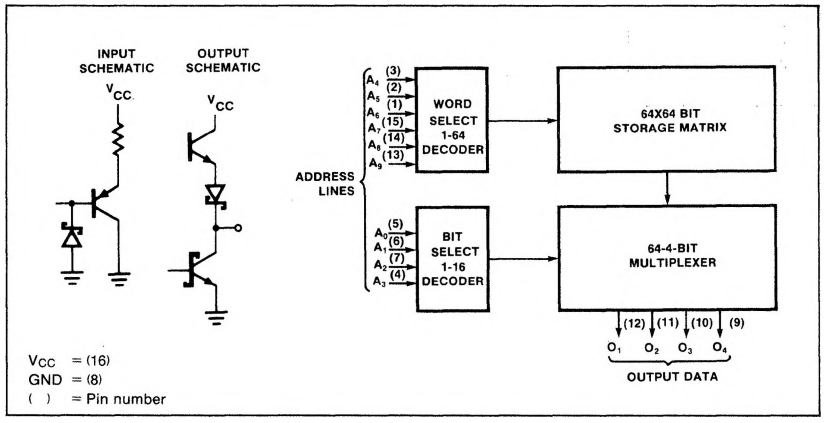
- **Microprogramming**
- **Hardwired algorithms**
- **Character recognition**
- **Character generation**
- **Control store**

PIN CONFIGURATION



*Dual-in-line (1/3 size of 24-pin package)

BLOCK DIAGRAM



DC ELECTRICAL CHARACTERISTICS $0°C \le T_A \le 75°C$, $4.75V \le V_{CC} \le 5.25V$

PARAMETER		TEST CONDITIONS	LIMITS			UNIT
			Min	Typ	Max	
	Input voltage					V
V_{IL}	Low				.85	
V_{IL}	High		2.0			
V_{IC}	Clamp	I_{IN} = -18mA	-1.2			
	Output voltage					V
V_{OL}	Low	I_{OUT} = 11.2mA			0.5	
V_{OH}	High	I_{OUT} = -1.0mA	2.7			
	Input current					μA
I_{IL}	Low	V_{IN} = 0.45V		-10	-400	
I_{IH}	High	V_{IN} = 5.5V		1	25	
	Output current					mA
I_{OS}	Short circuit	V_{OUT} = 0V	-20		-70	
I_{CC}	Power consumption	O_1 to O_3 = Low		140	170	mA

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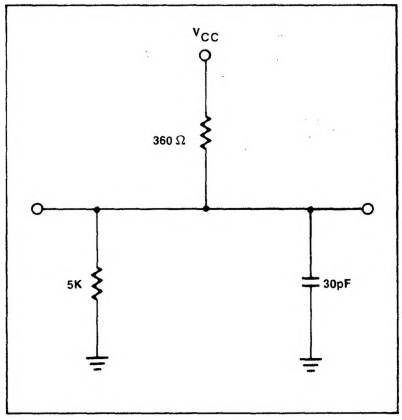
AC ELECTRICAL CHARACTERISTICS $0 \leq T_A \leq 75°C$, $4.75 \leq V_{CC} \leq 5.25V$

PARAMETER	TO	FROM	LIMITS			UNIT
			Min	Typ	Max	
Access time[1] T_{AA}	Output	Address		50	70	ns

NOTES

1. Rise and fall time for this test must be less than 5ns. Input amplitudes are 3.0V and all measurements are made at 1.5V.
2. Positive current is defined as into the terminal referenced.
3. No more than 1 output should be grounded at the same time.
4. Manufacturer reserves the right to make design and process changes and improvements.

TEST LOAD CIRCUIT



VOLTAGE WAVEFORM