

Philips Components—Signetics

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Memory Products	

# 82S09 82S09A

## 576-bit TTL bipolar RAM

### DESCRIPTION

The organization of this device allows byte storage of data, including parity. Where parity is not monitored, the ninth bit can be used as a tag or status indicator for each word stored. Ideal for scratch pad, push down stacks, buffer memories, and other internal memory applications in which cost and performance requirements dictate a wide data path in favor of word depth.

The 82S09/09A features Open-Collector outputs, Chip Enable input, and a very low current PNP input structure to enhance memory expansion.

Ordering codes are listed in the Ordering Information Table.

The 82S09 and 82S09A devices are also processed to military requirements for operation over the military temperature range. For specifications and ordering information consult the Signetics Military Data Handbook.

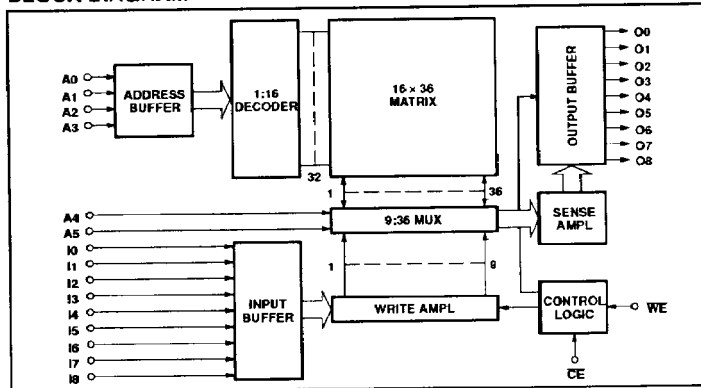
### FEATURES

- Address access time:
  - N82S09: 45ns max
  - N82S09A: 35ns max
- Write cycle time:
  - N82S09/09A: 45ns max
- Power dissipation: 1.3mW/bit typ
- Input loading: -100µA max
- On-chip address decoding
- Schottky clamped
- Fully TTL compatible
- Output is non-blanked during Write
- One Chip Enable input
- Outputs: Open-Collector

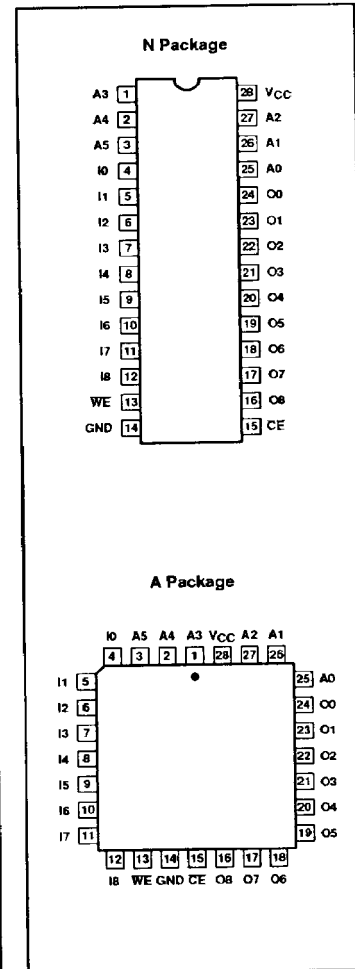
### APPLICATIONS

- Buffer memory
- Control register
- FIFO memory
- Push down stack
- Scratch pad

### BLOCK DIAGRAM



### PIN CONFIGURATIONS



**576-bit TTL bipolar RAM (64 × 9)****82S09 / 82S09A****ORDERING INFORMATION**

DESCRIPTION	ORDER CODE
28-Pin Plastic Dual-In-Line 600mil-wide	N82S09 N, N82S09A N
28-Pin Plastic Leaded Chip Carrier 450mil-square	N82S09 A, N82S09A A

**ABSOLUTE MAXIMUM RATINGS**

SYMBOL	PARAMETER	RATING	UNIT
$V_{CC}$	Supply voltage	+7.0	$V_{DC}$
$V_{IN}$	Input voltage	+5.5	$V_{DC}$
$V_{OH}$	Output voltage High	+5.5	$V_{DC}$
$T_{amb}$	Operating temperature range	0 to +75	°C
$T_{stg}$	Storage temperature range	-65 to +150	°C

**DC ELECTRICAL CHARACTERISTICS** $0^{\circ}\text{C} \leq T_{amb} \leq +75^{\circ}\text{C}$ ,  $4.75\text{V} \leq V_{CC} \leq 5.25\text{V}$ 

SYMBOL	PARAMETER	TEST CONDITIONS	LIMITS			UNIT
			MIN	TYP	MAX	
<b>Input voltage<sup>1</sup></b>						
$V_{IL}$	Low	$V_{CC} = 4.75\text{V}$	2.0		0.8	V
$V_{IH}$	High	$V_{CC} = 5.25\text{V}$			V	
$V_{IC}$	Clamp <sup>2</sup>	$V_{CC} = 4.75\text{V}$ , $I_{IN} = -12\text{mA}$			-1.5	V
<b>Output voltage<sup>1</sup></b>						
$V_{OL}$	Low <sup>3</sup>	$V_{CC} = 4.75\text{V}$ , $I_{OL} = 8.0\text{mA}$			0.5	V
<b>Input current</b>						
$I_{IL}$	Low	$V_{IN} = 0.45\text{V}$			-100	$\mu\text{A}$
$I_{IH}$	High	$V_{IN} = 5.5\text{V}$			25	$\mu\text{A}$
<b>Output current</b>						
$I_{OLK}$	Leakage <sup>4</sup>	$V_{CC} = 5.25\text{V}$ , $V_{OUT} = 5.5\text{V}$			40	$\mu\text{A}$
<b>Supply current<sup>5</sup></b>						
$I_{CC}$		$V_{CC} = 5.25\text{V}$			190	mA
<b>Capacitance</b>						
$C_{IN}$	Input	$V_{CC} = 5.0\text{V}$		5		pF
$C_{OUT}$	Output	$V_{IN} = 2.0\text{V}$ $V_{OUT} = 2.0\text{V}$		B		pF

**NOTES:**

- All voltage values are with respect to network ground.
- Test each input one at a time.
- Measured with the logic Low stored. Output sink current is applied through a resistor to  $V_{CC}$ .
- Measured with  $V_{IH}$  applied to CE.
- $I_{CC}$  is measured with the Write Enable and Chip Enable inputs grounded, all other inputs at 0.45V, and the outputs open.
- The operating ambient temperature ranges are guaranteed with transverse air flow exceeding 400 linear feet per minute and a 2-minute warm-up.

**TRUTH TABLE**

MODE	CE	WE	$I_N$	$O_N$
Read	0	1	X	Stored Data
Write "0"	0	0	0	1
Write "1"	0	0	1	0
Disable	1	X	X	1

X = Don't care

**576-bit TTL bipolar RAM (64 × 9)**

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**AC ELECTRICAL CHARACTERISTICS**

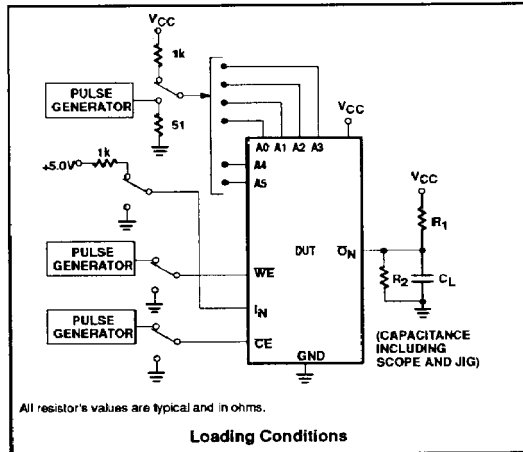
$R_1 = 600\Omega$ ,  $R_2 = 900\Omega$ ,  $C_L = 30\text{pF}$ ,  $0^\circ\text{C} \leq T_{\text{amb}} \leq +75^\circ\text{C}$ ,  $4.75\text{V} \leq V_{\text{CC}} \leq 5.25\text{V}$

SYMBOL	PARAMETER	TO	FROM	N82S09			N82S09A			UNIT
				MIN	TYP	MAX	MIN	TYP	MAX	
<b>Access time</b>										
$t_{\text{AA}}$	Address	Output	Address			45			35	ns
$t_{\text{CE}}$	Chip Enable	Output	Output			30			25	ns
<b>Disable time<sup>1</sup></b>										
$t_{\text{CD}}$	Valid time	Output	Chip Enable			30			25	ns
$t_{\text{WA}}$		Output	Write Enable			30			25	ns
<b>Setup and hold time</b>										
$t_{\text{WSA}}^2$	Setup time	Write Enable	Address	5			5			ns
$t_{\text{WHA}}$	Hold time	Write Enable	Address	5			5			ns
$t_{\text{WSD}}$	Setup time	Write Enable	Data in	35			30			ns
$t_{\text{WHD}}$	Hold time	Write Enable	Data in	5			5			ns
$t_{\text{WSC}}$	Setup time	Write Enable	CE	5			5			ns
$t_{\text{WHC}}$	Hold time	Write Enable	CE	5			5			ns
<b>Pulse width<sup>3</sup></b>										
$t_{\text{WP}}^4$	Write Enable			35			35			ns

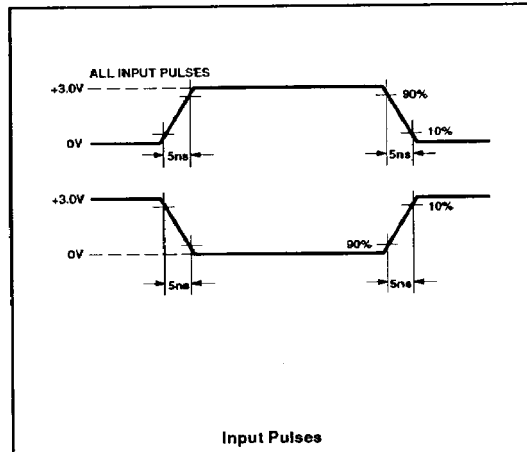
**NOTES:**

1. Measured at a delta of 0.5V from Logic level with  $R_1 = 750\Omega$ ,  $R_2 = 750\Omega$  and  $C_L = 5\text{pF}$ .
2. Measured with minimum  $t_{\text{WP}}$ .
3. Minimum required to guarantee a Write into the slowest bit.
4. Measured with minimum  $t_{\text{WSA}}$ .
5. The operating ambient temperature ranges are guaranteed with transverse air flow exceeding 400 linear feet per minute and a 2-minute warm-up.

**TEST LOAD CIRCUIT**



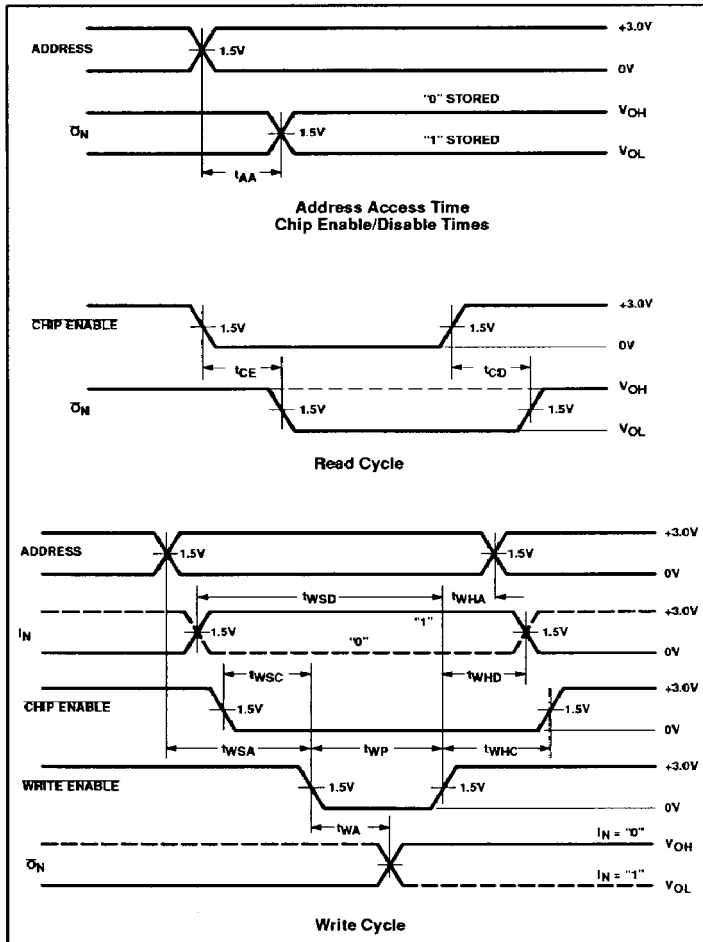
**VOLTAGE WAVEFORMS**



576-bit TTL bipolar RAM (64 × 9)

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TIMING DIAGRAMS



MEMORY TIMING DEFINITIONS

SYMBOL	PARAMETER
t <sub>CE</sub>	Delay between beginning of Chip Enable Low (with Address valid) and when Data Output becomes valid.
t <sub>CD</sub>	Delay between when Chip Enable becomes High and Data Output is in Off-State.
t <sub>AA</sub>	Delay between beginning of valid Address (with Chip Enable Low) and when Data Output becomes valid.
t <sub>WSC</sub>	Required delay between beginning of valid Chip Enable and beginning of Write Enable pulse.
t <sub>WHD</sub>	Required delay between end of Write Enable pulse and end of valid input data.
t <sub>WP</sub>	Width of Write Enable pulse.
t <sub>WSA</sub>	Required delay between beginning of valid Address and beginning of Write Enable pulse.
t <sub>WSD</sub>	Required delay between beginning of valid Data Input and end of Write Enable pulse.
t <sub>WHC</sub>	Required delay between end of Write Enable pulse and end of Chip Enable.
t <sub>WHA</sub>	Required delay between end of Write Enable pulse and end of valid Address.
t <sub>WR</sub>	Delay between end of Write Enable pulse and when Data Output becomes valid. (Assuming Address still valid.)
t <sub>WA</sub>	Delay between beginning of Write Enable pulse and when Data Output reflects complement of Data Input.