4-BIT SHIFT REGISTERS

82S70
82S71

ADVANCED INFORMATION

DIGITAL 8000 SERIES SCHOTTKY TTL/MSI

DESCRIPTION

The 82S70 is a 4-bit Shift Register with both serial and parallel data entry capability.

The data input lines are single-ended true input data lines which condition their specific register bit location after an enabled clocking transition. Since data transfer is synchronous with clock, data may be transferred in any serial/parallel input/output relationship.

Mode control logic is available to determine three possible control states. These register states are serial shift right mode, parallel enter mode, and no change or hold mode. These states accomplish logical decoding for system control.

The 82S71 provides a direct reset (R_D), and a $\overline{D_{out}}$ line in addition to the available outputs of the 82S70 element.

FEATURES

- SCHOTTKY-CLAMPED TTL STRUCTURE
- PNP INPUTS
- SYNCHRONOUS LOAD
- SHIFT RIGHT/LEFT CAPABILITY
- HOLD MODE

ELECTRICAL CHARACTERISTICS

Transfer Rate	60 MHz (Typ)
Input Load Current (Max)	
I_{In}"0"	400μA
I_{In}"1"	25μA
Output Current	
I_{out}"0"	20mA @ 0.5V
I_{out}"1"	1mA @ 2.7V

LOGIC DIAGRAM

82S70 AND 82S71