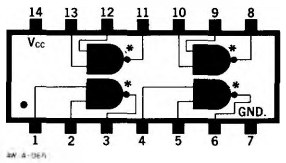
SIGNETICS DCL INTEGRATED CIRCUITS

8481 QUAD 2-INPUT NAND GATE

A PACKAGE



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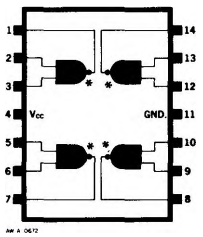


*No pull-up provided

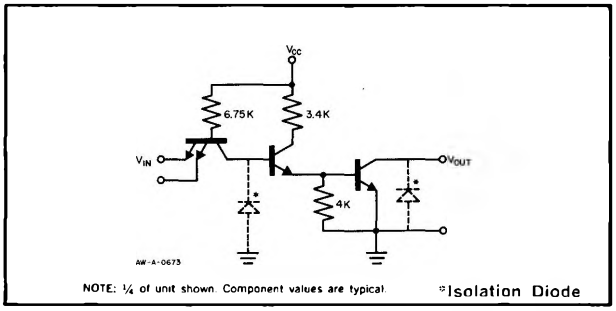
8481

The 8481 is a Quad 2-Input NAND Gate with bare output collectors. Absence of an output pull-up structure allows the user complete freedom in the use of the 8481 in collector-logic (wired-AND) and similar applications. Proper pull-up resistor selection will allow as many as 30 outputs to be tied together.

Collector logic, using the 8481, can provide increased system flexibility and lower system cost due to reduced can count.

Section 4 of this handbook provides detailed usage rules and collector-logic information for this element.

BASIC CIRCUIT SCHEMATIC



ELECTRICAL CHARACTERISTICS (NOTES: 1,2,3,4,5,6,12)

ACCEPTANCE TEST SUB-GROUP	CHARACTERISTIC	LIMITS				TEST CONDITIONS						
		MIN.	TYP.	MAX.	UNITS	TEMP. S8481	TEMP. N8481	V_{cc}	DRIVEN INPUT	OTHER INPUTS	OUTPUTS	NOTES
A-4	"1" OUTPUT LEAKAGE CURRENT			25	μA	+125°C	+75°C	5.0V	0.6V			11
A-5	"0" OUTPUT VOLTAGE			0.35	V	-55°C	0°C	4.75V	2.0V	2.0V	8.2mA	8
A-3				0.35	V	+25°C	+25°C	5.0V	2.0V	2.0V	8.2mA	8
A-4				0.35	V	+125°C	+75°C	4.75V	2.0V	2.0V	8.2mA	8
C-1	"0" INPUT CURRENT	-0.1		-0.8	mA	-55°C	0°C	5.25V	0.35V	5.25V		
A-3		-0.1		-0.8	mA	+25°C	+25°C	5.25V	0.35V	5.25V		
C-1		-0.1		-0.8	mA	+125°C	+75°C	5.25V	0.35V	5.25V		
A-4	"1" INPUT CURRENT			25	μA	+125°C	+75°C	5.0V	4.5V	0V		
A-6	PAIR DELAY	50		150	ns	+25°C	+25°C	5.0V			D.C. F.O. = 9	9,13
C-2	FALL TIME			75	ns	-55°C	0°C	4.75V			A.C. F.O. = 2	10,13
C-2	TURN-ON DELAY			40	ns	+25°C	+25°C	5.0V			D.C. F.O. = 9	9,13
C-2	TURN-OFF DELAY			50	ns	+25°C	+25°C	5.0V			D.C. F.O. = 1	9,13
C-2	INPUT CAPACITANCE			3.0	pf	+25°C	+25°C	5.0V	2.0V			7
A-2	POWER CONSUMPTION OUTPUT "0"			16.8	mW	+25°C	+25°C	5.25V				
	(Per Gate) OUTPUT "1"			5.2	mW	+25°C	+25°C	5.25V	0V			
A-2	INPUT VOLTAGE RATING	5.5			V	+25°C	+25°C	5.0V	50μA	0V		

Notes:

1. All voltage and capacitance measurements are referenced to the ground terminal. Terminals not specifically referenced are left electrically open.
2. All measurements are taken with ground pin tied to zero volts.
3. Positive current flow is defined as into the terminal referenced.
4. Positive NAND Logic definition: "UP" Level = "1", "DOWN" Level = "0".
5. Precautionary measures should be taken to ensure current limiting in accordance with Absolute Maximum Ratings should the isolation diodes become forward biased.
6. Measurements apply to each gate element independently.
7. Capacitance as measured on Boonton Electronic Corporation Model 75A-S8 Capacitance Bridge or equivalent. f = 1 MHz, V_{ac} = 25mV_{rms}. All pins not specifically referenced are tied to guard for capacitance tests. Output pins are left open.
8. Output sink current is supplied through a resistor to V_{cc}.
9. One DC fan-out is defined as 0.8mA.
10. One AC fan-out is defined as 50pf.
11. Connect an external 1K resistor from V_{cc} to the output terminal for this test.
12. Manufacturer reserves the right to make design and process changes and improvements.
13. Detailed test conditions for AC testing are in Section 3.