

**8808 SINGLE 8-INPUT NAND GATE**  
**8816 DUAL 4-INPUT NAND GATE**  
**8870 TRIPLE 3-INPUT NAND GATE**  
**8880 QUAD 2-INPUT NAND GATE**

These NAND gates provide high switching speed while maintaining high fan-out and noise margin. They perform the NAND function for positive logic (highest voltage level = "1") and the NOR function for negative logic (lowest voltage level = "1").

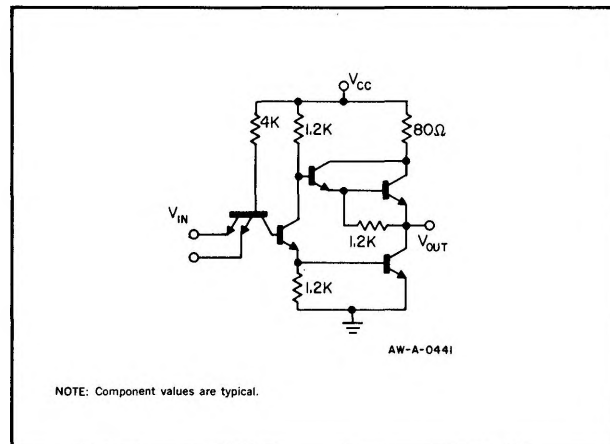
The output structure utilizes a totem-pole arrangement which employs a Darlington Pair for active pull-up. This configuration provides extremely low output impedance for the "1" output state. As a result, switching times are relatively insensitive to capacitive loads when compared to single transistor active pull-ups. The saturating output switching transistor provides a low impedance driving source in the output "0" state, enhancing turn-on times and providing high fan-out capability.

Because of the low output impedance of these gates, they exhibit high AC noise immunity at the output which is extremely important in high speed systems in eliminating erroneous cross-coupled signals.

Output short-circuit protection is provided by a current limiting resistor.

Section 4 of this handbook provides usage rules and application information for these gates.

**BASIC CIRCUIT SCHEMATIC**



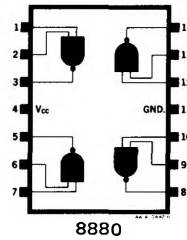
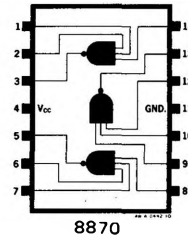
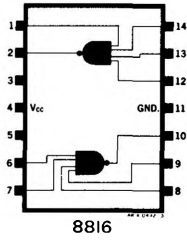
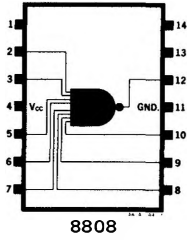
**ELECTRICAL CHARACTERISTICS (NOTES: 1, 2, 3, 4, 5, 6, 12)**

ACCEPTANCE TEST SUB-GROUP	CHARACTERISTIC	LIMITS				TEST CONDITIONS						
		MIN.	TYP.	MAX.	UNITS	TEMP. S8800	TEMP. N8800	V <sub>cc</sub>	DRIVEN INPUT	OTHER INPUTS	OUTPUTS	NOTES
A-5	"1" OUTPUT VOLTAGE	2.6			V	-55°C	0°C	4.75V	0.8V		-500μA	8
A-3		2.8			V	+25°C	+25°C	5.0V	0.8V		-500μA	8
A-4		2.6			V	+125°C	+75°C	4.75V	0.8V		-500μA	8
A-5	"0" OUTPUT VOLTAGE			0.40	V	-55°C	0°C	4.75V	2.0V	2.0V	16mA	9
A-3				0.40	V	+25°C	+25°C	5.0V	2.0V	2.0V	16mA	9
A-4				0.40	V	+125°C	+75°C	4.75V	2.0V	2.0V	16mA	9
C-1	"0" INPUT CURRENT	-0.1		-1.6	mA	-55°C	0°C	5.25V	0.40V	5.25V		
A-3		-0.1		-1.6	mA	+25°C	+25°C	5.25V	0.40V	5.25V		
C-1		-0.1		-1.6	mA	+125°C	+75°C	5.25V	0.40V	5.25V		
A-4	"1" INPUT CURRENT			25	μA	+125°C	+75°C	5.0V	4.5V	0V		
A-6	TURN-ON DELAY			13	ns	+25°C	+25°C	5.0V			D.C. F.O. = 20	10, 14
A-6	TURN-OFF DELAY			13	ns	+25°C	+25°C	5.0V			D.C. F.O. = 20	10, 14
C-2	OUTPUT FALL TIME			50	ns	-55°C	0°C	4.75V			A.C. F.O. = 6	11, 14
C-2	INPUT CAPACITANCE			3.0	pf	+25°C	+25°C	5.0V	2.0V			7
A-2	POWER CONSUMPTION "0"			31	mW	+25°C	+25°C	5.25V				
	(Per Gate)			8.9	mW	+25°C	+25°C	5.25V	0V			
C-1	INPUT LATCH VOLTAGE RATING	5.5			V	+25°C	+25°C	5.0V	10mA	0V		12
A-2	OUTPUT SHORT CIRCUIT CURRENT	-20		-70	mA	+25°C	+25°C	5.0V	0V		0V	

**Notes:**

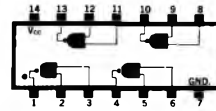
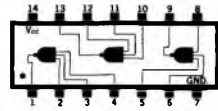
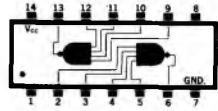
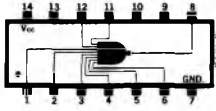
- All voltage and capacitance measurements are referenced to the ground terminal. Terminals not specifically referenced are left electrically open.
- All measurements are taken with ground pin tied to zero volts.
- Positive current flow is defined as into the terminal referenced.
- Positive NAND Logic definition: "UP" Level = "1", "DOWN" Level = "0".
- Precautionary measures should be taken to ensure current limiting in accordance with Absolute Maximum Ratings should the isolation diodes become forward biased.
- Measurements apply to each gate element independently.
- Capacitance as measured on Boonton Electronic Corporation Model 75A-S8 Capacitance Bridge or equivalent. f = 1MHz, V<sub>ac</sub> = 25mVrms. All pins not specifically referenced are tied to guard for capacitance tests. Output pins are left open.
- Output source current is supplied through a resistor to ground.
- Output sink current is supplied through a resistor to V<sub>cc</sub>.
- One DC fan-out is defined as 0.8mA.
- One AC fan-out is defined as 50pf.
- This test guarantees operation free of input latch-up over the specified operating supply voltage range.
- Manufacturer reserves the right to make design and process changes and improvements.
- Detailed test conditions for AC testing are in Section 3.

J PACKAGES



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A PACKAGE



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