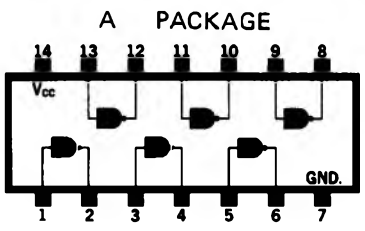
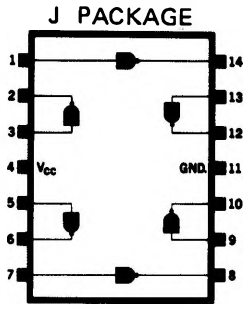
SIGNETICS DCL INTEGRATED CIRCUITS

# 8H90 HEX INVERTER

A PACKAGE




J PACKAGE




The 8H90 Hex Inverter is designed for ultra-high switching speed while maintaining high fan-out and noise margin.

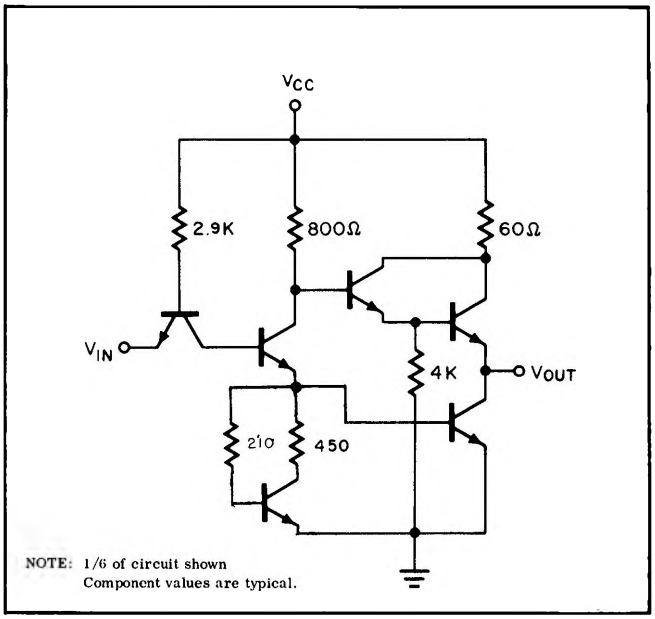
The output structure utilizes a totem-pole arrangement which employs a Darlington Pair for active pull-up. This configuration provides extremely low output impedance for the "1" output state. As a result, switching times are relatively insensitive to capacitive loads when compared to single transistor active pull-ups. The saturating output switching transistor provides a low impedance driving source in the output "0" state, enhancing turn-on times and providing high fan-out capability.

Because of the low output impedance of this element, it exhibits high AC noise immunity at the output which is extremely important in high speed systems in eliminating erroneous cross-coupled signals.

Output short circuit protection is provided by a current limiting resistor.

(Package drawings are on the reverse side.)

BASIC CIRCUIT SCHEMATIC




NOTE: 1/6 of circuit shown
Component values are typical.

## ELECTRICAL CHARACTERISTICS (NOTES: 1, 2, 3, 4, 5, 6, 13)

| ACCEPTANCE TEST SUB-GROUP | CHARACTERISTIC | LIMITS MIN. | TYP. | MAX. | UNITS | TEST CONDITIONS TEMP. S8H16 S8H70 S8H80 | TEMP. N8H16 N8H70 N8H80 | $V_{cc}$ | DRIVEN INPUT | OTHER INPUTS | OUTPUTS | NOTES |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| A-5 | "1" OUTPUT VOLTAGE | 2.6 | | | V | -55°C | 0°C | 4.75V | 0.8V | | -750μA | 8 |
| A-3 | | 2.8 | | | V | +25°C | +25°C | 5.00V | 0.8V | | -750μA | 8 |
| A-4 | | 2.6 | | | V | +125°C | +75°C | 4.75V | 0.8V | | -750μA | 8 |
| A-5 | "0" OUTPUT VOLTAGE | | | 0.4 | V | -55°C | 0°C | 4.75V | 2.0V | | 24mA | 9 |
| A-3 | | | | 0.4 | V | +25°C | +25°C | 5.00V | 2.0V | | 24mA | 9 |
| A-4 | | | | 0.4 | V | +125°C | +75°C | 4.75V | 2.0V | | 24mA | 9 |
| C-1 | "0" INPUT CURRENT | -0.1 | | -2.4 | mA | -55°C | 0°C | 5.25V | 0.4V | | | |
| A-3 | | -0.1 | | -2.4 | mA | +25°C | -25°C | 5.25V | 0.4V | | | |
| C-1 | | -0.1 | | -2.4 | mA | +125°C | +75°C | 5.25V | 0.4V | | | |
| A-4 | "1" INPUT CURRENT | | | 50 | μA | +125°C | +75°C | 5.00V | 4.5V | | | |
| | TURN-ON DELAY | | 7.0 | | ns | +25°C | +25°C | 5.00V | | | D.C. F.O. = 30 | 10, 14 |
| | TURN-ON DELAY | | 5.0 | | ns | +25°C | +25°C | 5.00V | | | D.C. F.O. = 3 | 10, 14 |
| | TURN-OFF DELAY | | 7.0 | | ns | +25°C | +25°C | 5.00V | | | D.C. F.O. = 30 | 10, 14 |
| | TURN-OFF DELAY | | 5.0 | | ns | +25°C | +25°C | 5.00V | | | D.C. F.O. = 3 | 10, 14 |
| C-2 | OUTPUT FALL TIME | | | 50 | ns | -55°C | 0°C | 4.75V | | | A.C F.O. = 6 | 11, 14 |
| | INPUT CAPACITANCE | | 2.0 | | pf | +25°C | +25°C | 5.00V | 2.0V | | | 7 |
| A-2 | POWER CONSUMPTION OUTPUT "0" | | | 46.2 | mW | +25°C | +25°C | 5.25V | | | | |
| | (Per Gate) OUTPUT "1" | | | 21.0 | mW | +25°C | +25°C | 5.25V | 0V | | | |
| C-1 | INPUT LATCH VOLTAGE RATING | 6.0 | | | V | +25°C | +25°C | 5.00V | 10mA | | | 12 |
| A-2 | OUTPUT SHORT CIRCUIT CURRENT | -40 | | -90 | mA | +25°C | +25°C | 5.00V | 0V | | 0V | |

## NOTES:

1. All voltage and capacitance measurements are referenced to the ground terminal. Terminals not specifically referenced are left electrically open.
2. All measurements are taken with ground pin tied to zero volts.
3. Positive current flow is defined as into the terminal referenced.
4. Positive NAND Logic definition: "UP" Level = "1", "DOWN" Level = "0".
5. Precautionary measures should be taken to ensure current limiting in accordance with Absolute Maximum Ratings should the isolation diodes become forward biased.
6. Measurements apply to each gate element independently.
7. Capacitance as measured on Boonton Electronic Corporation Model 75A-S8 Capacitance Bridge or equivalent. f = 1MHz, $V_{ac}$ = 25mV$_{rms}$. All pins not specifically referenced are tied to guard for capacitance tests. Output pins are left open.
8. Output source current is supplied through a resistor to ground.
9. Output sink current is supplied through a resistor to $V_{cc}$.
10. One DC fan-out is defined as 0.8mA.
11. One AC fan-out is defined as 50pf.
12. This test guarantees operation free of input latch-up over the specified operating supply voltage range.
13. Manufacturer reserves the right to make design and process changes and improvements.
14. Test conditions for AC testing are the same as for 8H80. See Section 3 of Signetics DCL Handbook.