QUAD BUS DRIVER/RECEIVER | 8T26

0°C TO +75°C

DIGITAL 8000 SERIES TTL/MSI

DESCRIPTION

The 8T26 bus driver/receiver contains four pair of inverting logic gates along with two buffered common enable lines.

Both the driver and receiver gates have tri-state outputs and PNP inputs. Tri-state outputs provide the high switching speeds of totem pole TTL circuits while offering the bus capability of open collector gates. PNP inputs reduce input loading to 200 μA maximum.

A logic "1" on the bus enable (B/E) input allows input data to be transferred to the output of the driver, while a logic "0" will force the output to a high impedance state and will also disable the PNP resulting in negligible input load current. The driver gate will sink 50mA of current with a maximum V_{CE} of 0.45V.

The receiver gate is enabled by a logic "0" on the input enable (I/E) pin and provides 16mA current sink capability;

FEATURES

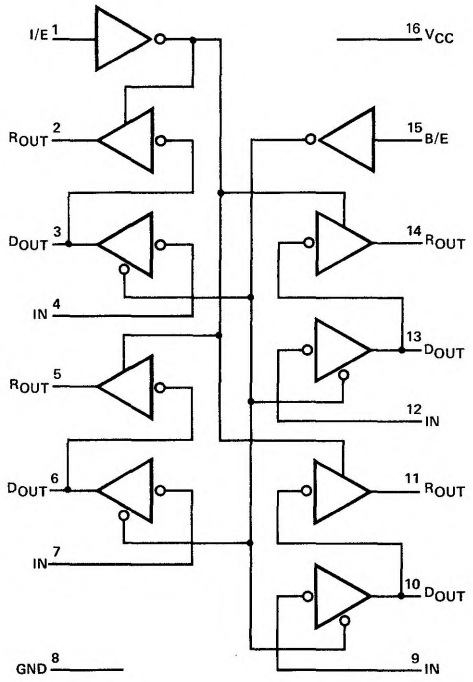
- SCHOTTKY-CLAMPED TTL
- PROPAGATION DELAY = 17nS (MAX.)
- TRI-STATE OUTPUTS
- PNP INPUTS
- 40mA CURRENT SINK CAPABILITY
- SBD* INPUT CLAMPS

*SCHOTTKY-BARRIER-DIODE

APPLICATIONS

- HALF-DUPLEX DATA TRANSMISSION
- ROUTING DATA IN BUS-ORIENTED SYSTEMS
- HIGH CURRENT DRIVERS

LOGIC DIAGRAM



V_{CC} = (16)
GND = (8)
( ) = Denotes Pin Numbers

ELECTRICAL CHARACTERISTICS (V_{CC} = 5.0V ±5%, T_A = 0°C to 75°C)

SYMBOL	PARAMETER	MIN.	TYP.	MAX.	UNITS	CONDITION
$I(0)_{in}$	Input "0" current (All Inputs)			−200	μA	V_{in} = 0.4
$I(1)_{in}$	Input "1" current Pins 1, 4, 7, 9, 12, 15			25	μA	V_{in} = 5.25
$V(0)_{in}$	Input (0) Threshold voltage	0.85			Volts	
$V(1)_{in}$	Input (1) Threshold voltage			2	Volts	
$V(1)_{out}$	Output (1) voltage Pins 3, 6, 10, 13	2.6	3.3		Volts	I_{out} = −10.0mA
$V(1)_{out}$	Output (1) voltage Pins 2, 5, 11, 14	2.6	3.3		Volts	I_{out} = −2.0mA
$V(0)_{out}$	Output (0) voltage Pins 3, 6, 10, 13		0.2	0.45	Volts	I_{out} = 50mA
$V(0)_{out}$	Output (0) voltage Pins 2, 5, 11, 14		0.2	0.45	Volts	I_{out} = 16mA
$I(1)_{off}$	Output (1) off/Leakage current			100	μA	V_{out} = 2.6V
$I(0)_{off}$	Output (0) off/Leakage current			−100	μA	V_{out} = 0.45V
V_{cin}	Input/Clamp/Voltage			−1.0	Volts	I_{in} = −5mA
I_{so}	Output (1) short circuit current - - Pins 3, 6, 10, 13	−50		−150	mA	V_o = 0 Volts*
I_{so}	Output (1) short circuit current - - Pins 2, 5, 11, 14	−30		−75	mA	V_o = 0 Volts*
I_{CC}	Power supply current			80	mA	V_{CC} = 5V

T_A = 25°C, V_{CC} = 5.00V

SYMBOL	PARAMETER	MIN.	TYP.	MAX.	UNITS	CONDITION
T_{on}	Turn on delay Pins 2, 5, 11, 14			10	nsec	30 pF, 300 ohm
T_{off}	Turn off delay Pins 2, 5, 11, 14			15	nsec	30 pF, 300 ohm
T_{on}	Turn on delay Pins 3, 6, 10, 13			17	nsec	150 pF, 100 ohm
T_{off}	Turn off delay Pins 3, 6, 10, 13			17	nsec	150 pF, 100 ohm

*Do not ground more than one output at a time.

TYPICAL APPLICATION

BI DIRECTIONAL DATA BUS