SIGNETICS DCL INTEGRATED CIRCUITS

8T80 QUAD 2-INPUT NAND INTERFACE GATE
8T90 HEX INVERTER INTERFACE ELEMENT

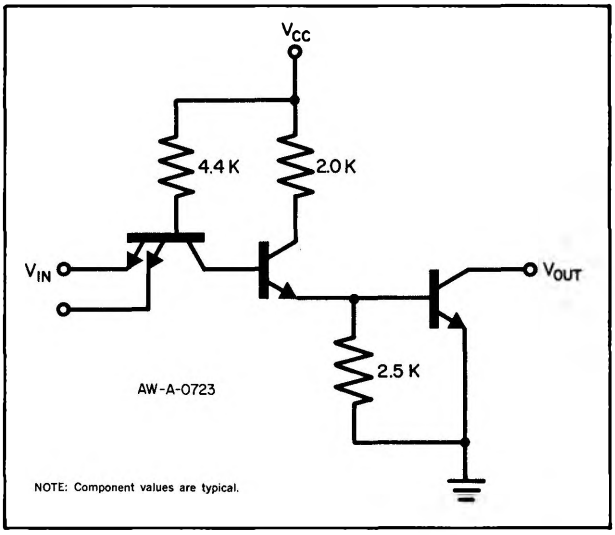
The 8T80 Quad 2-Input NAND Interface Gate and the 8T90 Hex Inverter Interface Element are low to high voltage elements which provide translation from standard logic levels of 5 volts to voltage levels of up to 30 volts.

The 8T80 performs the NAND function for positive logic (highest voltage level = "1") and the 8T90 performs the inverting function.

The output structure of each element features a high voltage transistor with bare collector which allows logic swings up to 30 volts. The bare collector allows collector logic or wired-AND to be easily implemented.

Usage and applications information for these devices is included in Section 4 of this handbook.

BASIC CIRCUIT SCHEMATIC



NOTE: Component values are typical.

ELECTRICAL CHARACTERISTICS (NOTES: 1, 2, 3, 4, 5, 6, 10, 12)

ACCEPTANCE TEST SUB-GROUP	CHARACTERISTIC	LIMITS				TEST CONDITIONS						
		MIN.	TYP.	MAX.	UNITS	TEMP. S8T80 S8T90	TEMP. N8T80 N8T90	V_{cc}	DRIVEN INPUT	OTHER INPUTS	OUTPUTS	NOTES
A-4	"1" OUTPUT LEAKAGE CURRENT			100	μA	+125°C	+75°C	5.0V	0.6V			7
A-5	"0" OUTPUT VOLTAGE			1.0	V	-55°C	0°C	4.75V	2.0V	2.0V	20mA	8
A-3				1.0	V	+25°C	+25°C	5.0V	2.0V	2.0V	20mA	8
A-4				1.0	V	+125°C	+75°C	4.75V	2.0V	2.0V	20mA	8
C-1	"0" OUTPUT VOLTAGE			0.35	V	-55°C	0°C	4.75V	2.0V	2.0V	7.2mA	8,9
C-1				0.35	V	+25°C	+25°C	5.0V	2.0V	2.0V	7.2mA	8,9
C-1				0.35	V	+125°C	+75°C	4.75V	2.0V	2.0V	7.2mA	8,9
C-1	"0" INPUT CURRENT	-0.1		-1.6	mA	-55°C	0°C	5.25V	0.35V	5.25V		
A-3		-0.1		-1.6	mA	+25°C	+25°C	5.25V	0.35V	5.25V		
C-1		-0.1		-1.6	mA	+125°C	+75°C	5.25V	0.35V	5.25V		
A-4	"1" INPUT CURRENT			25	μA	+125°C	+75°C	5.0V	4.5V	0V		
A-6	TURN-ON DELAY		35	55	ns	+25°C	+25°C	5.0V				13
A-6	STORAGE TIME		40	95	ns	+25°C	+25°C	5.0V				13
A-2	POWER CONSUMPTION OUTPUT "0"			20.0	mW	+25°C	+25°C	5.25V				
A-2	(Per Gate) OUTPUT "1"			7.9	mW	+25°C	+25°C	5.25V	0V			
A-2	INPUT VOLTAGE RATING	6.0			V	+25°C	+25°C	5.0V	50μA	0V		
A-2	OUTPUT VOLTAGE RATING	40			V	+25°C	+25°C	5.0V	0V			11

Notes:

1. All voltage and capacitance measurements are referenced to the ground terminal. Terminals not specifically referenced are left electrically open.
2. All measurements are taken with ground pin tied to zero volts.
3. Positive current flow is defined as into the terminal referenced.
4. Positive NAND Logic definition: "UP" Level = "1", "DOWN" Level = "0".
5. Precautionary measures should be taken to ensure current limiting in accordance with Absolute Maximum Ratings should the isolation diodes become forward biased.
6. Measurements apply to each gate element independently.
7. Output leakage current is supplied through a 2KΩ resistor to 30V.
8. Output sink current is supplied through a resistor to 30V.
9. This test applies to 8T90 only.
10. "OTHER INPUTS" applies to 8T80 only.
11. For this test, connect a 2KΩ resistor from output under test to 41V and a 10pf capacitor from output to ground.
12. Manufacturer reserves the right to make design and process changes and improvements.
13. Detailed test conditions for AC testing are in Section 3.

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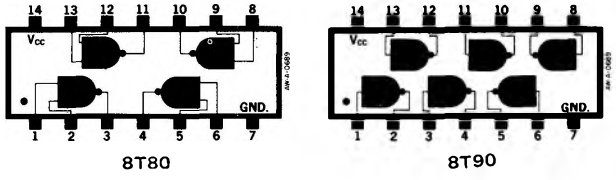

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