## 9310 • 9316 93L10 • 93L16 93S10 • 93S16 BCD DECADE COUNTER/ 4-BIT BINARY COUNTER

DESCRIPTION - The '10 is a high speed synchronous BCD decade counter and the ' 16 is a high speed synchronous 4 -bit binary counter. They are synchronously presetable, multifunctional MSI building blocks useful in a large number of counting, digital integration and conversion applications. Several states of synchronous operation are obtainable with no external gating packages required through an internal carry lookahead counting technique.

- SYNCHRONOUS COUNTING AND PARALLEL ENTRY
- DECODED TERMINAL COUNT
- BUILT-IN CARRY CIRCUITRY
- EASY INTERFACING WITH DTL, LPDTL, AND TTL FAMILIES

ORDERING CODE: See Section 9


INPUT LOADING/FAN-OUT: See Section 3 for U.L. definitions

'16, 'L16



FUNCTIONAL DESCRIPTION - The '10 counts modulo-10 in the BCD (8421) sequence. From state 9 (HLLH) it increments to state 0 (LLLL). The '16 counts modulo-16 in binary sequence. From state 15 (HHHH) it increments to state 0 (LLLL). The clock inputs of all flip-flops are driven in parallel through a clock buffer. Thus all changes of the Q outputs (except due to Master Reset) occur as a result of, and synchronous with, the LOW-to-HIGH transition of the CP input signal. The circuits have four fundamental modes of operation, in order of precedence: asynchronous reset, parallel load, count-up and hold. Four control inputs - Master Reset ( $\overline{\mathrm{MR}}$ ) Parallel Enable ( $\overline{\mathrm{PE}}$ ), Count Enable Parallel (CEP) and Count Enable Trickle (CET) - determine the mode of operation, as shown in the Mode Select Table. A LOW signal on $\overline{M R}$ overrides all other inputs and asynchronously forces all outputs LOW. A LOW signal on $\bar{P} E$ overrides counting and allows information on the Parallel Data $\left(P_{n}\right)$ inputs to be loaded into the flip-flops on the next rising edge of CP. With $\overline{P E}$ and $\overline{M R}$ HIGH, CEP and CET permit counting when both are HIGH. Conversely, a LOW signal on either CEP or CET inhibits counting.

The TTL and LP-TTL versions ('10, '16, 'L10 and 'L16 as opposed to the 'S10 and 'S16) contain masterslave flipflops which are "next-state catching" because of the JK feedback. This means that when CP is LOW, information that would change the state of a flip-flop, whether from the counting logic or the parallel entry logic if either mode is momentarily enabled, enters the master and is locked in. Thus to avoid inadvertently changing the state of a master latch, and the subsequent transfer of the erroneous information to the slave when the clock rises, it is necessary to insure that neither the counting mode, nor the parallel entry mode is momentarily enabled while CP is LOW. The S-TTL versions ('S10 and 'S16) use D-type edge-triggered flip-flops and changing the $\overline{P E}$, CEP and CET inputs when the CP is in either state does not cause errors, provided that the recommended setup and hold times, with respect to the rising edge of $C P$, are observed.

The Terminal Count (TC) output is HIGH when CET is HIGH and the counter is in its maximum count state (9 for the decade counters, 15 for the binary counters - fully decoded in both types). To implement synchronous multistage counters, the TC outputs can be used with the CEP and CET inputs in two different ways. These two schemes are shown in Figures a and b. The TC output is subject to decoding spikes due to internal race conditions and is therefore not recommended for use as a clock or asynchronous reset for flip-flops, counters or registers. If a decade counter is preset to an illegal state, or assumes an illegal state when power is applied, it will return to the normal sequence within two counts, as shown in the state diagrams.

Multistage Counting - The '10/'16 counters may be cascaded to provide multistage synchronous counting. Two methods commonly used to cascade these counters are shown in Figures a and b.

In multistage counting, all less significant stages must be at their terminal count before the next more significant counter is enabled. The ' $10 / 16$ internally decodes the terminal count condition and "ANDs" it with the CET input to generate the terminal count (TC) output. This arrangement allows one to perform series enabling by connecting the TC output (enable signal) to the CET input of the following stage, Figure a. The setup requires very few interconnections, but has the following drawback: since it takes time for the enable to ripple through the counter stages, there is a reduction in maximum counting speed. To increase the counting rate, it is necessary to decrease the propagation delay of the TC signal, which is done in the second method.

The scheme illustrated in Figure $b$ permits multistage counting, limited by the fan-out of the terminal count. The CEP input of the '10/'16 is internally "ANDed" with the CET input and as a result, both must be HIGH for the counter to be enabled. The CET inputs are connected as before except for the second stage. There the CET input is left floating and is therefore HIGH. Also, all CEP inputs are connected to the terminal output of the first stage. The advantage of this method is best seen by assuming all stages except the second and last are in their terminal condition. As the second stage advances to its terminal count, an enable is allowed to trickle down to the last counter stage, but has the full cycle time of the first counter to reach it. Then as the TC of the first stage goes active (HIGH), all CEP inputs are activated, allowing all stages to count on the next clock.

MODE SELECT TABLE

| INPUTS |  |  |  |  | RESPONSE |
| :---: | :---: | :---: | :---: | :---: | :---: |
| $\overline{\mathrm{MR}}$ | $\overline{\text { PE }}$ | CEP | CET |  |  |
| L | X | X | X | x | Clear; All Outputs LOW |
| H | L | X | X | ת | Parallel Load; $\mathrm{P}_{\mathbf{n}} \longrightarrow \mathrm{Q}_{\mathbf{n}}$ |
| H | H | L | X | X | Hold |
| H | H | X | L | x | Hold; TC = LOW |
| H | H | H | H | - | Count Up |

$H=$ HIGH Voltage Level
$L=$ LOW Voltage Level
$X=$ Immaterial

## LOGIC EQUATIONS

Count Enable $=$ MR $\bullet P E \cdot C E P \cdot C E T$
Terminal Count $=$ CET $\bullet Q_{0} \bullet Q_{1} \bullet Q_{2} \bullet Q_{3}$ ('16)
Terminal Count $=$ CET $\bullet \mathrm{Q}_{0} \bullet \overline{\mathrm{Q}}_{1} \bullet \overline{\mathrm{Q}}_{2} \bullet \mathrm{Q}_{3} \quad(' 10)$

STATE DIAGRAMS

'10, 'L10

'16, 'S16, 'L16


NOTE: The ' 20 can be preset to any state, but will not count beyond 9 . If preset to state $10,11,12,13,14$ or 15 , it will return to its normal sequence within two clock pulses.


Fig. a Synchronous Multistage Counting Scheme (Slow)


Fig. b Synchronous Multistage Counting Scheme (Fast)

| SYMBOL | PARAMETER | 93XX |  | 93L | 935 | UNITS | CONDITIONS |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: |
|  |  | Min | Max | Min Max | Min Max |  |  |
| Ios | Output Short Circuit Current | -20 | -80 | -2.5 -25 | -40 -100 | mA | $\mathrm{Vcc}=$ Max |
| Icc | Power Supply Current |  | 92 | 27.5 | 127 | mA | $\begin{aligned} & V_{c c}=M a x, \\ & M R=G n d \end{aligned}$ |
| AC CHARACTERISTICS: $\mathrm{VCC}=+5.0 \mathrm{~V}, \mathrm{~T}_{\mathrm{A}}=+25^{\circ} \mathrm{C}$ (See Section 3 for waveforms and load configurations) |  |  |  |  |  |  |  |
| SYMBOL | PARAMETER | 93XX |  | 93L | 935 | UNITS | CONDITIONS |
|  |  | $C_{L}=15 \mathrm{pF}$ |  | $C_{L}=15 \mathrm{pF}$ | $C_{L}=15 \mathrm{pF}$ |  |  |
|  |  | Min | Max | Min Max | Min Max |  |  |
| ${ }^{\text {max }}$ | Maximum Count Frequency | 30 |  | 13 | 70 | MHz |  |
| $\left\lvert\, \begin{aligned} & \text { tPLH } \\ & \text { tPHL } \\ & \hline \end{aligned}\right.$ | Propagation Delay CP to Q |  | $\begin{aligned} & 20 \\ & 23 \end{aligned}$ | $\begin{aligned} & 32 \\ & 39 \end{aligned}$ | $\begin{array}{r} 9.0 \\ 13 \end{array}$ | ns | Figs. 3-1, 3-8 |
| $\left\lvert\, \begin{aligned} & \text { tPLH } \\ & \text { tPHL } \\ & \hline \end{aligned}\right.$ | Propagation Delay CP to TC |  | $\begin{aligned} & 35 \\ & 22 \\ & \hline \end{aligned}$ | $\begin{aligned} & 66 \\ & 30 \end{aligned}$ | $\begin{aligned} & 18 \\ & 12 \end{aligned}$ | ns |  |
| $\left\lvert\, \begin{aligned} & \text { tPLH } \\ & \text { tPHL } \\ & \hline \end{aligned}\right.$ | Propagation Delay CET to TC |  | $\begin{aligned} & 19 \\ & 19 \end{aligned}$ | $\begin{aligned} & 35 \\ & 30 \end{aligned}$ | $\begin{aligned} & \hline 10 \\ & 10 \end{aligned}$ | ns | Figs. 3-1, 3-5 |
| tPHL | Propagation Delay $\overline{M R}$ to $Q$ |  | 45 | 62 | 20 | ns | Figs. 3-1, 3-16 |

AC OPERATING REQUIREMENTS: $\mathrm{V}_{\mathrm{C}} \mathrm{C}=+5.0 \mathrm{~V}, \mathrm{~T}_{\mathrm{A}}=+25^{\circ} \mathrm{C}$

| SYMBOL | PARAMETER | 93XX |  | 93L |  | 935 |  | UNITS | CONDITIONS |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: |
|  |  | Min | Max | Min | Max | Min | Max |  |  |
| $\begin{aligned} & \mathrm{ts}_{s}(\mathrm{H}) \\ & \mathrm{ts}_{s}(\mathrm{~L}) \end{aligned}$ | Setup Time HIGH or LOW $P_{n}$ to CP | $\begin{aligned} & 30 \\ & 30 \end{aligned}$ |  | $\begin{aligned} & 75 \\ & 75 \end{aligned}$ |  | $\begin{aligned} & 8.0 \\ & 5.0 \end{aligned}$ |  | ns | Fig. 3-6 |
| $\begin{aligned} & \operatorname{tn}(H) \\ & \operatorname{tn}(L) \end{aligned}$ | Hold Time HIGH or LOW $P_{n}$ to CP | $\begin{aligned} & 0 \\ & 0 \end{aligned}$ |  | $\begin{aligned} & 10 \\ & 10 \\ & \hline \end{aligned}$ |  | 0 |  | ns |  |
| $\begin{aligned} & \text { ts (H) } \\ & \text { t (L) } \end{aligned}$ | Setup Time HIGH or LOW PE to CP | Note 30 |  | Note 2 53 |  | $\begin{array}{r} 10 \\ 5.0 \end{array}$ |  | ns | Fig. 3-6 |
| $\begin{aligned} & \operatorname{tn}(H) \\ & \operatorname{tn}(L) \end{aligned}$ | Hold Time HIGH or LOW $\overline{P E}$ to CP | $-7.0$ <br> Note |  | $7.0$ <br> Note 2 |  | 0 |  | ns |  |
| $\begin{aligned} & \text { ts (H) } \\ & \text { ts (L) } \end{aligned}$ | Setup Time HIGH or LOW CEP or CET to CP | $\begin{gathered} 22 \\ \text { Note } 1 \\ \hline \end{gathered}$ |  | $\begin{array}{\|c\|} \hline 26 \\ \text { Note } 1 \\ \hline \end{array}$ |  | $\begin{aligned} & 9.0 \\ & 7.5 \\ & \hline \end{aligned}$ |  | ns | Fig. 3-6 |
| $\begin{aligned} & \text { th (H) } \\ & \text { th (L) } \end{aligned}$ | Hold Time HIGH or LOW CEP or CET to CP | $\begin{gathered} \text { Note } \\ 0 \end{gathered}$ |  | $\begin{gathered} \text { Note } \\ 10 \end{gathered}$ |  | 0 |  | ns |  |
| $\begin{array}{ll} \mathrm{tw}_{w}(H) \\ \mathrm{t}_{\mathrm{w}}(\mathrm{~L}) \end{array}$ | CP Pulse Width | $\begin{aligned} & 17 \\ & 17 \end{aligned}$ |  | $\begin{aligned} & 25 \\ & 25 \end{aligned}$ |  | $\begin{aligned} & 6.5 \\ & 7.0 \end{aligned}$ |  | ns | Fig. 3-8 |
| tw (L) | $\overline{M R}$ Pulse Width LOW | 30 |  | 65 |  | 14 |  | ns | Fig. 3-16 |
| trec | Recovery Time $\overline{M R}$ to CP | 15 |  | 55 |  | 5.5 |  | ns | Fig. 3-16 |
| NOTES: <br> (1) The Setup Time "t (L)"and Hold Time "th ( H )" between the Count Enable (CEP and CET) and the Clock (CP) indicate that the HIGH-to-LOW transition of the CEP and CET must occur only while the Clock is HIGH for conventional operation. <br> (2) The Setup Time "ts ( $H$ )" and Hold Time "th ( L " between the Parallel Enable ( $\overline{\mathrm{PE}}$ ) and Clock (CP) indicate that the LOW-to-HIGH transition of the PE must occur only while the Clock is HIGH for conventional operation. |  |  |  |  |  |  |  |  |  |

