Stereo Audio, 24-Bit, 96 kHz, Multibit Σ-Δ ADC

AD1871

FEATURES

- 5.0 V Stereo Audio ADC
  - with 3.3 V Tolerant Digital Interface
- Supports 96 kHz Sample Rates
- Supports 16-/20-/24-Bit Word Lengths
- Multibit Sigma-Delta Modulators with
  - "Perfect Differential Linearity Restoration" for Reduced Idle Tones and Noise Floor
- 105 dB (Typ) Dynamic Range
- Supports 256/512 and 768 × f_S Master Clocks
- Flexible Serial Data Port
  - Allows Right-Justified, Left-Justified, I^2S Compatible and DSP Serial Port Modes
  - Cascadable (up to Four Devices) from a Single DSP SPORT
- Device Control via SPI Compatible Serial Port or
  - Optional Control Pins
- On-Chip Reference
- 28-Lead SSOP Package

APPLICATIONS

- Professional Audio
- Mixing Consoles
- Musical Instruments
- Digital Audio Recorders, Including
  - CD-R, MD, DVD-R, DAT, HDD
- Home Theater Systems
- Automotive Audio Systems
- Multimedia

PRODUCT OVERVIEW

The AD1871 is a stereo audio ADC intended for digital audio applications requiring high performance analog-to-digital conversion. It features two 24-bit conversion channels each with programmable gain amplifier (PGA), multibit sigma-delta modulator, and decimation filters. Each channel provides 105 db of dynamic range, making the AD1871 suitable for applications such as digital audio recorders and mixing consoles.

Each of the AD1871's input channels (left and right) can be configured as either differential or single-ended (two inputs muxed with internal single-ended-to-differential conversion). The input PGA features a gain range of 0 dB to 12 dB in steps of 3 dB. The Σ-Δ modulator features a proprietary multibit architecture that realizes optimum performance over an audio bandwidth with standard audio sampling rates of 32 kHz up to 96 kHz. The decimation filter response features very low pass-band ripple and excellent stop-band attenuation.

The AD1871's audio data interface supports all common interface formats such as I^2S, left-justified, right-justified as well as other modes that allow for convenient connection to general-purpose digital signal processors (DSPs). The AD1871 also features an SPI compatible serial control port that allows for convenient control of device parameters and functionality such as sample word-width, PGA settings, interface modes, and so on.

The AD1871 operates from a single 5 V power supply—with an optional digital interfacing capability of 3.3 V. It is housed in a 28-lead SSOP package and is characterized for operation over the temperature range –40°C to +105°C.

FUNCTIONAL BLOCK DIAGRAM

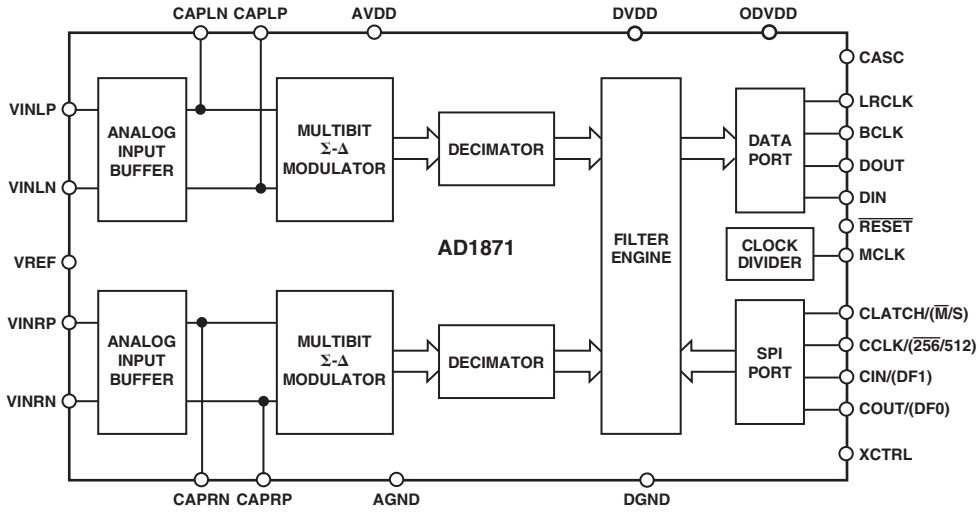

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TABLE OF CONTENTS

AD1871–SPECIFICATIONS

TEST CONDITIONS UNLESS OTHERWISE NOTED

Supply Voltages . . . . . 5.0 V
Ambient Temperature . . . . . 25°C
Input Clock (f_{CLKIN}) [$256 \times f_S$] . . . . . 12.288 MHz
Input Signal . . . . . 991.768 Hz
. . . . . –0.5 dB Full Scale (dBFS) (Differential, PGA/MUX Enabled)
Measurement Bandwidth . . . . . 23.2 Hz to 19.998 kHz
Word Width . . . . . 24 Bits
Load Capacitance on Digital Outputs . . . . . 100 pF
Input Voltage High (V_{IH}) . . . . . 2.4 V
Input Voltage Low (V_{IL}) . . . . . 0.8 V
Master Mode, Data I^2S Justified

ANALOG PERFORMANCE

Parameter	Min	Typ	Max	Unit	Conditions
RESOLUTION		24		Bits	
DIFFERENTIAL INPUT					PGA/MUX Enabled
Dynamic Range					(20 Hz to 20 kHz, –60 dB Input)
Unweighted	98	103		dB	
A-Weighted	100	105		dB	
Signal-to-Noise Ratio		106		dB	
Total Harmonic Distortion + Noise		–85		dB	Input = –0.5 dBFS
(THD+N)		–103		dB	Input = –20 dBFS
Multibit Modulator Only					Modulator Output @ 5.6448 MHz
Dynamic Range (A-Weighted)		102		dB	
SINGLE-ENDED INPUT					PGA/MUX Enabled
Dynamic Range					(20 Hz to 20 kHz, –60 dB Input)
Unweighted		103		dB	
A-Weighted		105		dB	
Signal-to-Noise Ratio		106		dB	
Total Harmonic Distortion + Noise		–85		dB	Input = –0.5 dBFS
(THD+N)		–103		dB	Input = –20 dBFS
DIFFERENTIAL INPUT (BYPASS)					PGA/MUX Disabled
Dynamic Range					(20 Hz to 20 kHz, –60 dB Input)
Unweighted		103		dB	
A-Weighted		106		dB	
Signal-to-Noise Ratio		106		dB	
Total Harmonic Distortion + Noise		–86		dB	Input = –0.5 dBFS
(THD+N)		–104		dB	Input = –20 dBFS
DIFFERENTIAL INPUT (f_S = 96 kHz)					PGA/MUX Enabled; AMC = 1
Dynamic Range					(20 Hz to 20 kHz, –60 dB Input)
Unweighted		103		dB	
A-Weighted		106		dB	
Signal-to-Noise Ratio		106		dB	
Total Harmonic Distortion + Noise		–87		dB	Input = –0.5 dBFS
(THD+N)		–104		dB	Input = –20 dBFS
Analog Inputs					
Differential Input Range (± Full Scale)	–2.828		+2.828	V	
Input Impedance (PGA/MUX)		8		kΩ	Differential
Input Impedance (ByPass)		40		kΩ	Differential
Input Impedance (PGA/MUX)		4		kΩ	Single Ended
V_{REF}	2.138	2.25	2.363	V	
DC Accuracy					
Gain Error		–10		%	
Interchannel Gain Mismatch	–0.2	–0.01	+0.2	dB	
Gain Drift		100		ppm/°C	
Crosstalk (EIAJ Method)		–100		dB	

LOW-PASS DIGITAL FILTER CHARACTERISTICS (f_S = 48 kHz)

Parameter	Min	Typ	Max	Unit
Decimation Factor		128		
Pass-Band Frequency		21.77		kHz
Stop-Band Frequency		26.23		kHz
Pass-Band Ripple		±0.01		dB
Stop-Band Attenuation		120		dB
Group Delay		910		µs

LOW-PASS DIGITAL FILTER CHARACTERISTICS (f_S = 96 kHz)

Parameter	Min	Typ	Max	Unit
Decimation Factor		64		
Pass-Band Frequency		43.54		kHz
Stop-Band Frequency		52.46		kHz
Pass-Band Ripple		±0.01		dB
Stop-Band Attenuation		120		dB
Group Delay		460		µs

HIGH-PASS DIGITAL FILTER CHARACTERISTICS (f_S = 48 kHz)

Parameter	Min	Typ	Max	Unit
Cutoff Frequency		2		Hz

HIGH-PASS DIGITAL FILTER CHARACTERISTICS (f_S = 96 kHz)

Parameter	Min	Typ	Max	Unit
Cutoff Frequency		4		Hz

MASTER CLOCK (MCLK) AND RESET TIMING

Mnemonic	Description	Min	Typ	Max	Unit	Comment
t_{MCH}	MCLK High Width	20			ns	
t_{MCL}	MCLK Low Width	20			ns	
t_{PDR}	$\overline{\text{RESET}}$ Low Pulsewidth	20			ns	

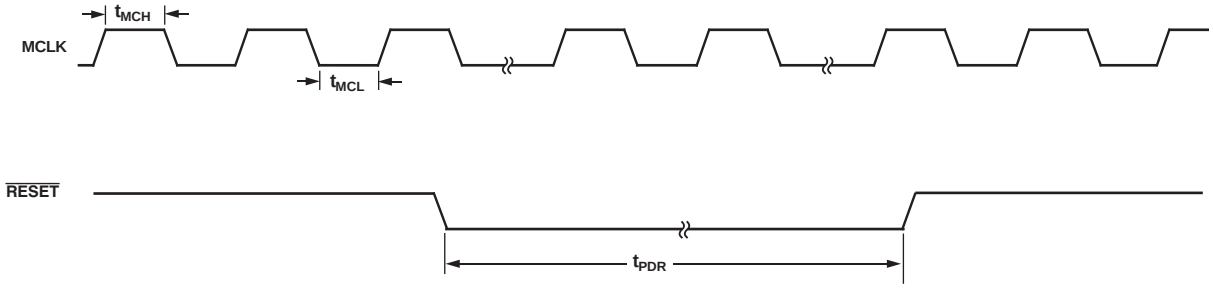


Figure 1. MCLK/$\overline{\text{RESET}}$ Timing

DATA INTERFACE TIMING (STANDALONE MODE–MASTER)

Mnemonic	Description	Min	Typ	Max	Unit	Comment
t_{BDLY}	BCLK Delay	20			ns	From MCLK Rising
t_{BLDLY}	LRCLK Delay to Low	10			ns	From BCLK Falling
t_{BDDLY}	DOUT Delay	10			ns	From BCLK Falling

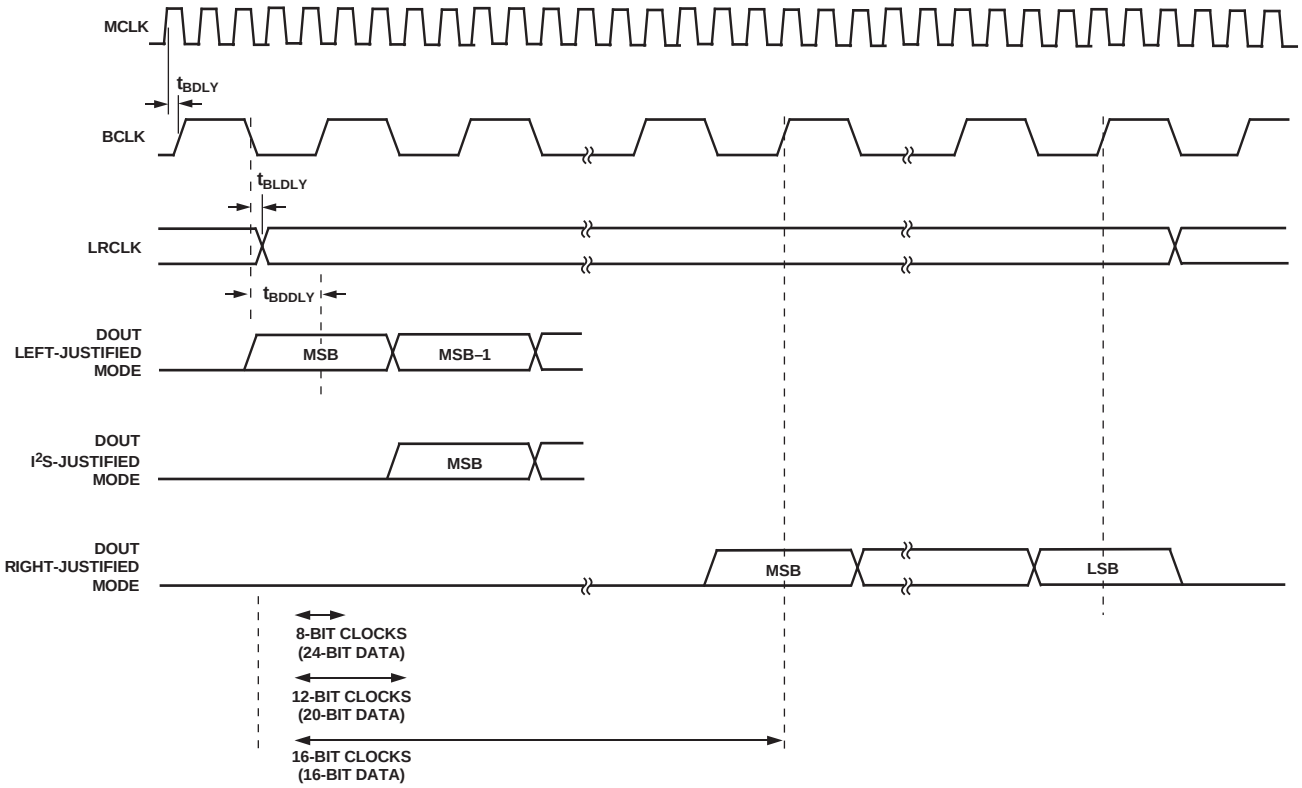


Figure 2. Master Data Interface Timing

DATA INTERFACE TIMING (STANDALONE MODE–SLAVE)

Mnemonic	Description	Min	Typ	Max	Unit	Comment
t_{BCH}	BCLK High Width		30		ns	
t_{BCL}	BCLK Low Width		30		ns	
t_{BDSD}	DOUT Delay	20			ns	From BCLK Falling
t_{LRS}	LRCLK Setup	10			ns	To BCLK Rising
t_{LRH}	LRCLK Hold	5			ns	From BCLK Rising

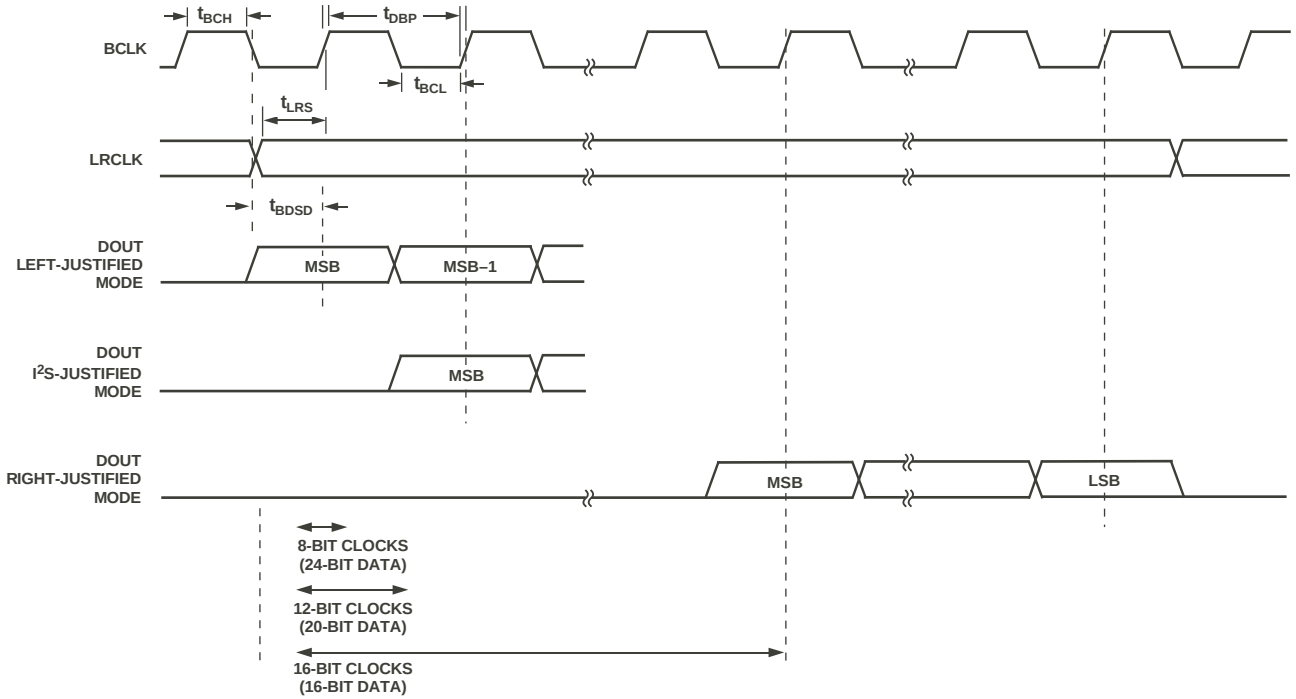


Figure 3. Slave Data Interface Timing

DATA INTERFACE TIMING (CASCADE MODE–MASTER)

Mnemonic	Description	Min	Typ	Max	Unit	Comment
t_{BCHDC}	BCLK High Delay	20			ns	From MCLK Rising
t_{BCLDC}	BCLK Low Delay	20			ns	From MCLK Falling
t_{BLRDC}	LRCLK Delay	10			ns	From BCLK Rising
t_{BDDC}	DOUT Delay	10			ns	From BCLK Rising
t_{BDIS}	DIN Setup	10			ns	To BCLK Rising
t_{BDIH}	DIN Hold	10			ns	From BCLK Rising

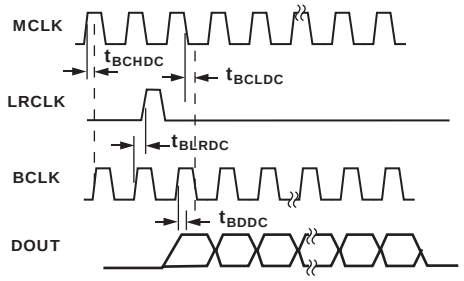


Figure 4. Master Cascade Interface Timing

DATA INTERFACE TIMING (CASCADE MODE–SLAVE)

Mnemonic	Description	Min	Typ	Max	Unit	Comment
t_{BCHC}	BCLK High Width		30		ns	
t_{BCLC}	BCLK Low Width		30		ns	
t_{BDSDC}	DOUT Delay	20			ns	From BCLK Rising
t_{LRSC}	LRCLK Setup	10			ns	To BCLK Rising
t_{LRHC}	LRCLK Hold	5			ns	From BCLK Rising
t_{BDIS}	DIN Setup	10			ns	To BCLK Rising
t_{BDIH}	DIN Hold	10			ns	From BCLK Rising

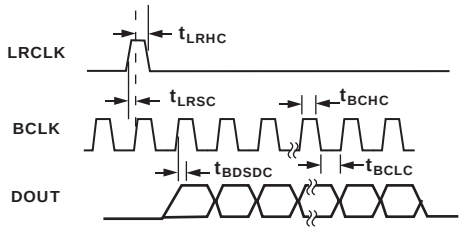


Figure 5. Slave Cascade Interface Timing

DATA INTERFACE TIMING (MODULATOR MODE)

Mnemonic	Description	Min	Typ	Max	Unit	Comment
t_{MOCH}	MODCLK High Width		MCLK		ns	
t_{MOCL}	MODCLK Low Width		MCLK		ns	
t_{MHDD}	MOD DATA High Delay		30		ns	From MCLK Rising
t_{MLDD}	MOD DATA Low Delay		20		ns	From MCLK Falling
t_{MMDR}	MODCLK Delay Rising		30		ns	MCLK Falling to MODCLK Rising
t_{MMDF}	MODCLK Delay Falling		20		ns	MCLK Falling to MODCLK Falling

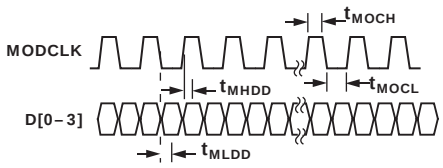


Figure 6. Modulator Mode Timing

CONTROL INTERFACE (SPI) TIMING

Mnemonic	Description	Min	Typ	Max	Unit	Comment
t_{CCH}	CCLK High Width	40			ns	
t_{CCL}	CCLK Low Width	40			ns	
t_{CCP}	CCLK Period	80			ns	
t_{CDS}	CDATA Setup Time	10			ns	To CCLK Rising
t_{CDH}	CDATA Hold Time	10			ns	From CCLK Rising
t_{CLS}	CLATCH Setup Time	10			ns	To CCLK Rising
t_{CLH}	CLATCH Hold Time	10			ns	From CCLK Rising
t_{COE}	COUT Enable	15			ns	From CLATCH Falling
t_{COD}	COUT Delay	20			ns	From CCLK Falling
t_{COTS}	COUT Three-State	25			ns	From CLATCH Rising

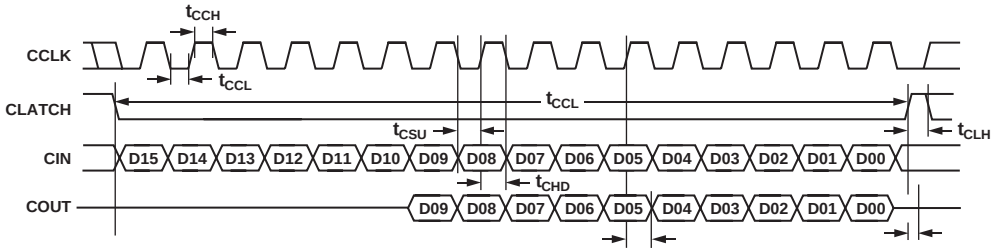


Figure 7. Control Interface Timing

DIGITAL I/O

Parameter	Min	Typ	Max	Unit
Input Voltage High (V_{IH})	2.4			V
Input Voltage Low (V_{IL})			0.8	V
Input Leakage (I_{IH} @ V_{IH} = 5 V)			10	µA
Input Leakage (I_{IL} @ V_{IL} = 0 V)			10	µA
Output Voltage High (V_{OH} @ I_{OH} = –2 mA)	ODVDD – 0.4 V			V
Output Voltage Low (V_{OL} @ I_{OL} = +2 mA)			0.4	V
Input Capacitance			15	pF

POWER

Parameter	Min	Typ	Max	Unit
Supplies				
Voltage, AVDD, and DVDD	4.5	5	5.5	V
Voltage, ODVDD	2.7		5.5	V
Analog Current		40	45	mA
Analog Current—Power-Down (MCLK Running)		4.0	6.0	µA
Digital Current, DVDD		18	22	mA
Digital Current, ODVDD		0.5	1.0	mA
Digital Current—Power-Down (MCLK Running) DVDD*		0.8	2.0	mA
Digital Current—Power-Down (MCLK Running) ODVDD*		1.0	15.0	µA
Power Supply Rejection				
1 kHz 300 mV p-p Signal at Analog Supply Pins		–86		dB
20 kHz 300 mV p-p Signal at Analog Supply Pins		–77		dB

*$\overline{\text{RESET}}$ held low.

TEMPERATURE RANGE

Parameter	Min	Typ	Max	Unit
Specifications Guaranteed		25		°C
Functionality Guaranteed	–40		+105	°C
Storage	–65		+150	°C

Specifications subject to change without notice.

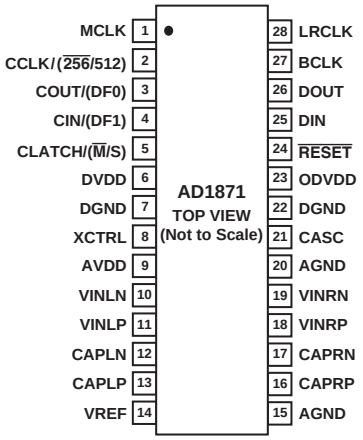
ABSOLUTE MAXIMUM RATINGS

	Min	Typ	Max	Unit
DVDD to DGND and ODVDD to DGND	0		6	V
AVDD to AGND	0		6	V
Digital Inputs	DGND – 0.3		DVDD + 0.3	V
Analog Inputs	AGND – 0.3		AVDD + 0.3	V
AGND to DGND	–0.3		+0.3	V
Reference Voltage		Indefinite Short Circuit to Ground		
Soldering (10 sec)			300	°C

ORDERING GUIDE

Model	Temperature	Package Description	Package Option
AD1871YRS	–40°C to +105°C	SSOP	RS-28
AD1871YRS-REEL	–40°C to +105°C	SSOP	RS-28 in 13″ Reel (1500 pieces)
EVAL-AD1871EB		Evaluation Board	

PIN CONFIGURATION



CAUTION

ESD (electrostatic discharge) sensitive device. Electrostatic charges as high as 4000 V readily accumulate on the human body and test equipment and can discharge without detection. Although the AD1871 features proprietary ESD protection circuitry, permanent damage may occur on devices subjected to high energy electrostatic discharges. Therefore, proper ESD precautions are recommended to avoid performance degradation or loss of functionality.

PIN FUNCTION DESCRIPTIONS

Pin No.	Input/ Output	Mnemonic	Description
1	I	MCLK	Master Clock. The master clock input determines the sample rate of the device. MCLK can be 256, 512, or 768 times the sampling frequency.
2	I	CCLK[1]	Control Port Bit Clock—clock signal for control port (SPI) interface. This pin is reconfigured in the External Control Mode (Pin XCTRL is high), see below.
3	I/O	COUT[1, 2]	Control Port Data Out—serial data output from the control port (SPI) interface (in readback). This pin is reconfigured in the External Control Mode (Pin XCTRL is high), see below; or in Modulator Mode (Bit MME of Control Register II is set), see below.
4	I	CIN[1]	Control Port Data Input—serial data input for control port (SPI) interface. This pin is reconfigured in the External Control Mode (Pin XCTRL is high), see below.
5	I	CLATCH[1]	Control Port Frame Sync—frame sync (framing signal) for control port (SPI) interface. This pin is reconfigured in the External Control Mode (Pin XCTRL is high), see below.
6	I	DVDD	5 V Digital Core Supply
7	I	DGND	Digital Ground
8	I	XCTRL	External Control Enable. This pin is used to select the Control Mode for the device. When XCTRL is low, control is via the SPI compatible control port (Pins CCLK, CLATCH, CIN, and COUT). When XCTRL is enabled (high), control of several device functions is possible by hardware pin strapping (Pins $\overline{256}$/512, $\overline{M}$/S, DF1, and DF0). In External Control Mode, all other functions are in default state (please refer to the Control Register Descriptions and External Control section).
9	I	AVDD	5 V Analog Supply
10	I	VINLN	Left Channel, Negative Input (via MUX/PGA)
11	I	VINLP	Left Channel, Positive Input (via MUX/PGA)
12	I/O	CAPLN	Left External Filter Capacitor (Negative Input to Modulator)
13	I/O	CAPLP	Left External Filter Capacitor (Positive Input to Modulator)
14	O	VREF	Reference Voltage Output. It is recommended to connect a capacitor combination of 10 µF in parallel with 0.1 µF between VREF and AGND (Pin 15). (See Layout Recommendations.)
15	I	AGND	Analog Ground
16	I/O	CAPRP	Right External Filter Capacitor (Positive Input to Modulator)
17	I/O	CAPRN	Right External Filter Capacitor (Negative Input to Modulator)
18	I	VINRP	Right Channel, Positive Input (via MUX/PGA)
19	I	VINRN	Right Channel, Negative Input (via MUX/PGA)
20	I	AGND	Analog Ground
21	I	CASC	Cascade Enable. This pin enables cascading of up to four AD1871 devices to a single DSP serial port (see Cascading section).
22	I	DGND	Digital Ground
23	I	ODVDD	Digital Interface Supply. The digital interface can operate from 3.3 V to 5.0 V (nominal).
24	I	$\overline{\text{RESET}}$	Reset
25	I/O	DIN[2]	Serial Data Input. Serial data input pin, only valid when the device is configured in Cascade Mode (Pin CASC is high). This pin is reconfigured in Modulator Mode (Bit MME of Control Register II is set), see below.
26	O	DOUT[2]	Audio Serial Data Output. This pin is reconfigured in Modulator Mode (Bit MME of Control Register II is set), see below.
27	I/O	BCLK[2]	Audio Serial Bit Clock. The bit clock is the audio data serial clock and determines the rate of audio data transfer. This pin is reconfigured in Modulator Mode (Bit MME of Control Register II is set), see below.
28	I/O	LRCLK[2]	Left/Right Clock. This clock, also known as the word clock, determines the sampling rate. It is an output or input depending on the status of $\overline{\text{Master}}$/Slave. This pin is reconfigured in Modulator Mode (Bit MME of Control Register II is set), see below.

NOTES
[1]External Control Mode (See pg 11)
[2]Modulator Mode (See pg 11)

Pin Function Redefinition in External Control Mode

Pin No.	Input/ Output	Mnemonic	Description
2	I	$\overline{256}$/512	Clock Rate Select. This pin is used to select between an MCLK of 256 × f_S (pin low) or 512 × f_S (pin high).
3	I	DF0	Data Format Select 0. This pin is used as the low bit (DF0) of the data format selection (see section on External Control).
4	I	DF1	Data Format Select 1. This pin is used as the high bit (DF1) of the data format selection (see section on External Control).
5	I	$\overline{M}$/S	Master/Slave Select. This pin is used to select between the Master (pin low) or Slave (pin high) Modes.

Pin Function Redefinition in Modulator Mode

Pin No.	Input/ Output	Mnemonic	Description
3	O	MODCLK	This pin provides a clock output that allows the user to decode the left and right channel modulator outputs. It is similar to a left/right clock but runs (nominally) at 5.6448 MHz and gates a 4-bit modulator output word in each phase (see section on Modulator Mode).
25	O	D3	Bit 3 of the Modulator Output Word
26	O	D2	Bit 2 of the Modulator Output Word
27	O	D1	Bit 1 of the Modulator Output Word
28	O	D0	Bit 0 of the Modulator Output Word

TERMINOLOGY

Dynamic Range

The ratio of a full-scale input signal to the integrated input noise in the pass band (20 Hz to 20 kHz), expressed in decibels (dB). Dynamic range is measured with a –60 dB input signal and is equal to (S/[THD+N]) + 60 dB. Note that spurious harmonics are below the noise with a –60 dB input, so the noise level establishes the dynamic range. The dynamic range is specified with and without an A-Weight filter applied.

Signal to (Total Harmonic Distortion + Noise) (S/[THD+N])

The ratio of the root-mean-square (rms) value of the fundamental input signal to the rms sum of all other spectral components in the pass band, expressed in decibels (dB).

Pass Band

The region of the frequency spectrum unaffected by the attenuation of the digital decimator's filter.

Pass-Band Ripple

The peak-to-peak variation in amplitude response from equal-amplitude input signal frequencies within the pass band, expressed in decibels.

Stop Band

The region of the frequency spectrum attenuated by the digital decimator's filter to the degree specified by stop-band attenuation.

Gain Error

With a near full-scale input, the ratio of the actual output to the expected output, expressed as a percentage.

Interchannel Gain Mismatch

With identical near full-scale inputs, the ratio of the outputs of the two stereo channels, expressed in decibels.

Gain Drift

Change in response to a near full-scale input with a change in temperature, expressed as parts-per-million (ppm) per °C.

Crosstalk (EIAJ Method)

Ratio of response on one channel with a grounded input to a full-scale 1 kHz sine-wave input on the other channel, expressed in decibels.

Power Supply Rejection

With no analog input, signal present at the output when a 300 mV p-p signal is applied to power supply pins, expressed in decibels of full scale.

Group Delay

Intuitively, the time interval required for an input pulse to appear at the converter's output, expressed in milliseconds (ms). More precisely, the derivative of radian phase with respect to radian frequency at a given frequency.

GLOSSARY

ADC—Analog-to-Digital Converter

DSP—Digital Signal Processor

IMCLK—Internal master clock signal, used to clock the decimating filter section. (Its frequency must be $256 \times f_S$.)

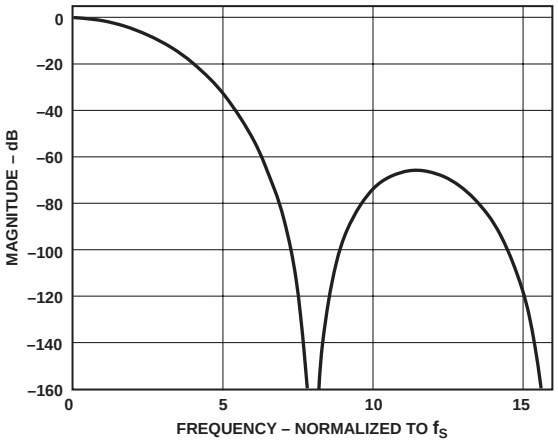
MCLK—External master clock signal applied to the AD1871. Its frequency can be 256, 512, or $768 \times f_S$. MCLK is divided internally to give an IMCLK frequency that must be $256 \times f_S$.

MODCLK—This is the Σ-Δ modulator clock that determines the sample rate of the modulator. Ideally, it should not exceed the lower of 6.144 MHz or $128 \times f_S$. The MODCLK is derived from the IMCLK by a divider that can be selected as /2 or /4.

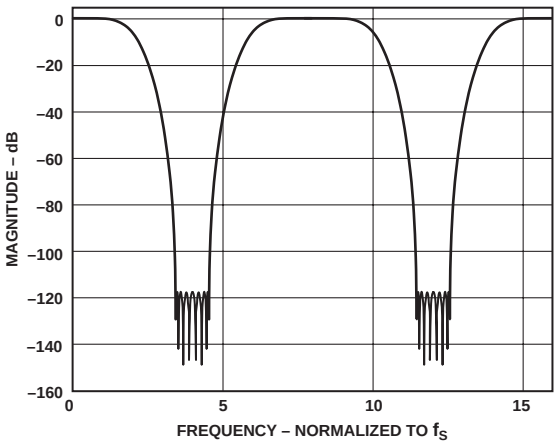
MUX—Multiplexer

PGA—Programmable Gain Amplifier

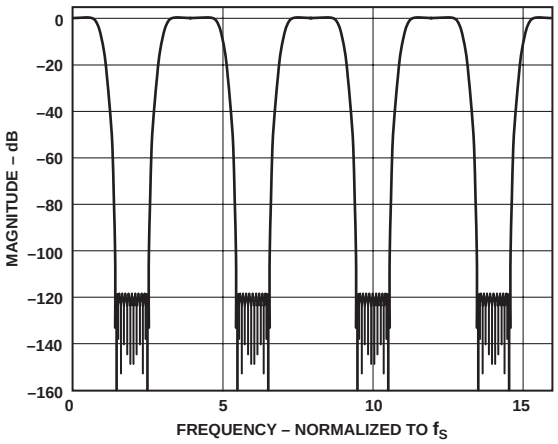
FILTER RESPONSES



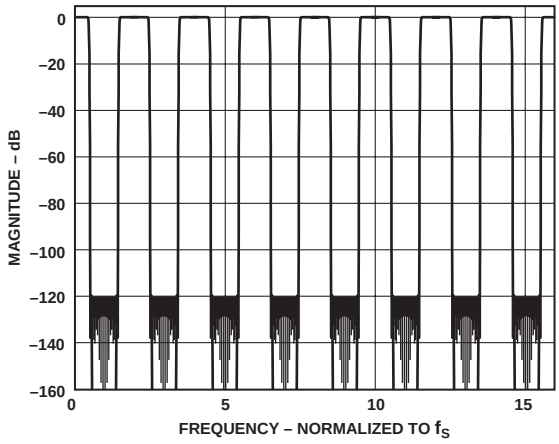
TPC 1. Sinc Filter Response (AMC = 0)



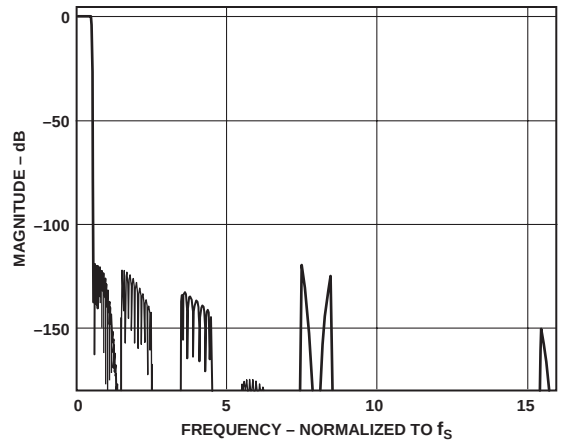
TPC 2. First Half-Band Filter Response



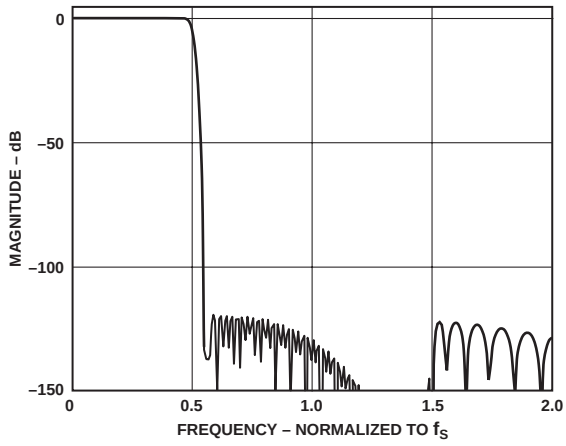
TPC 3. Comb Compensation Filter Response



TPC 4. Second Half-Band Filter Response

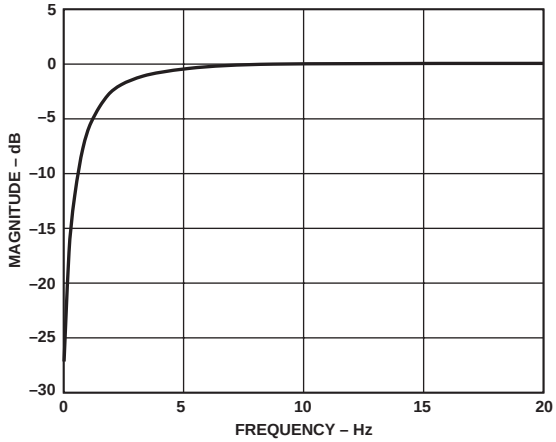


TPC 5. Composite Filter Response (AMC = 0)

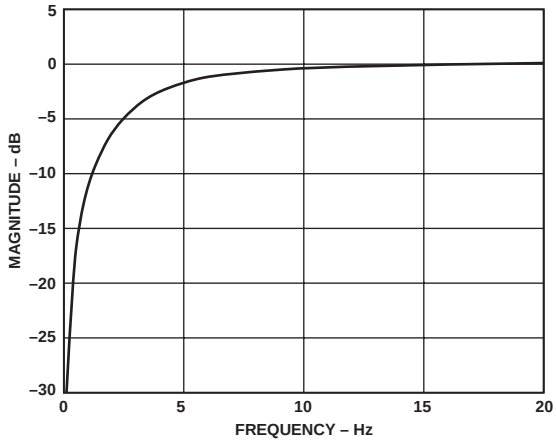


TPC 6. Composite Filter Response (Pass Band Section) (AMC = 0)

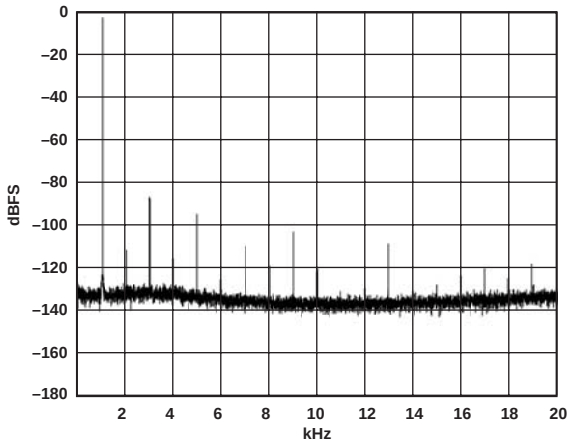
DEVICE PERFORMANCE CURVES



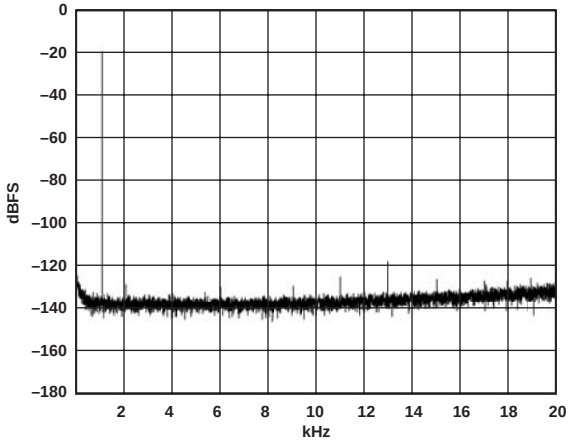
TPC 7. High-Pass Filter Response, f_S = 48 kHz



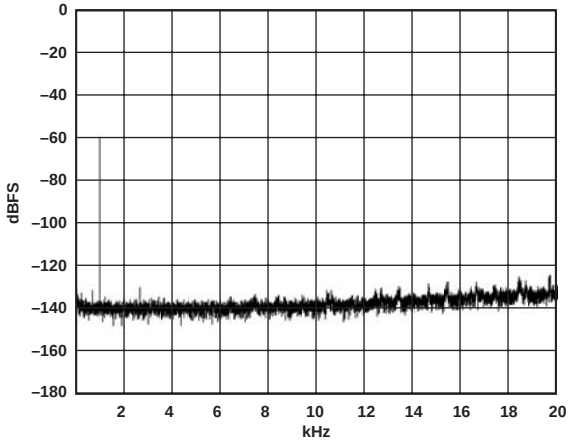
TPC 8. High-Pass Filter Response, f_S = 96 kHz



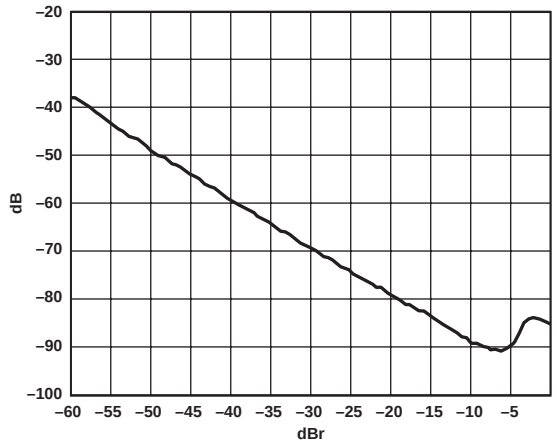
TPC 9. 1 kHz Tone at –0.5 dBFS, (32 k-Point FFT), f_S = 48 kHz



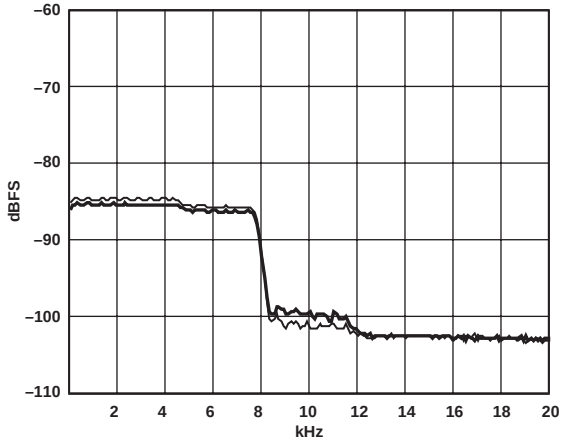
TPC 10. 1 kHz Tone at –20 dBFS, (32 k-Point FFT), f_S = 48 kHz



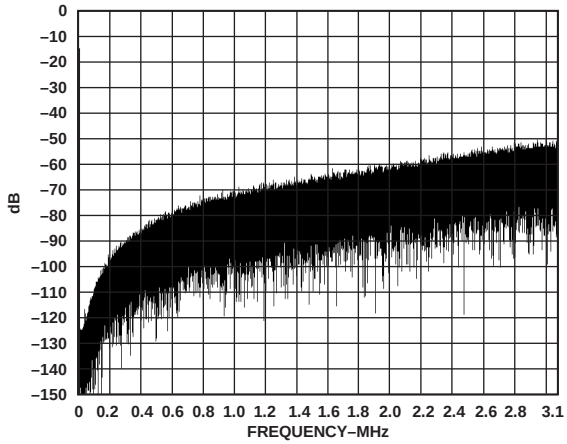
TPC 11. 1 kHz Tone at –60 dBFS, (32 k-Point FFT), f_S = 48 kHz



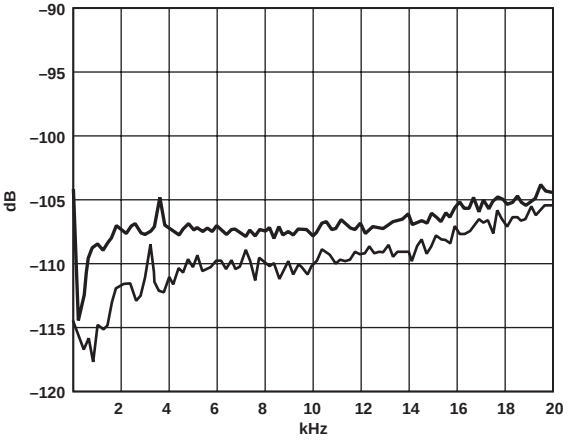
TPC 12. THD+N vs. Input Amplitude at 1 kHz, f_S = 48 kHz



TPC 13. THD+N vs. Input Frequency at –0.5 dBFS, f_S = 48 kHz



TPC 15. FFT of Modulator Output at –0.5 dBFS, f_S = 6.144 MHz



TPC 14. Channel Separation vs. Frequency at –0.5 dBFS, f_S = 48 kHz

FUNCTIONAL DESCRIPTION

Clocking Scheme

The MCLK pin is the input for the master clock frequency to the device. Nominally the MCLK frequency will be $256 \times f_S$ for correct operation of the device. However, if the user's MCLK is a multiple of $256 \times f_S$ (perhaps $512 \times f_S$ or $768 \times f_S$), it is possible to divide down the MCLK frequency to a suitable internal master clock frequency (IMCLK) using the MCLK divider block as shown in Figure 8. The divide options can be chosen from pass-through (/1), /2, or /3 corresponding with $256 \times f_S$, $512 \times f_S$, or $768 \times f_S$ MCLKs, respectively. The MCLK divider can be controlled using the MCD1–MCD0 Bits of Control Register III. (see Table XIII.)

The resulting internal MCLK (IMCLK) is used to run the decimating and filtering engine and must be chosen to be at a ratio of $256 \times f_S$.

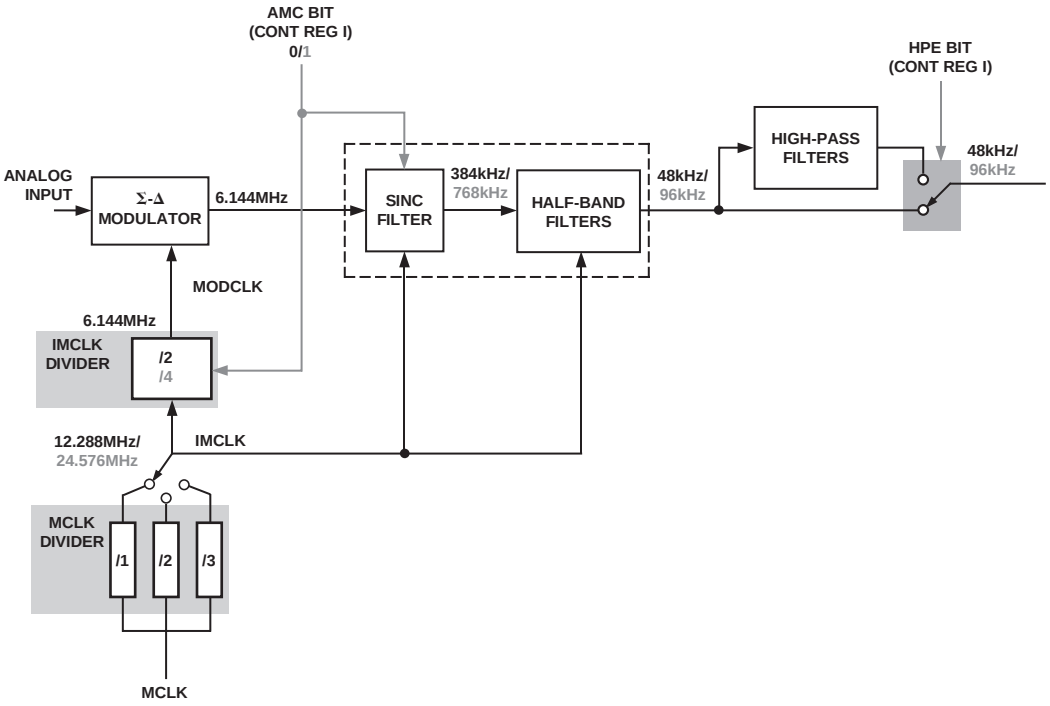


Figure 8. Clocking Scheme to Modulator and Filter Engine

Modulator

The AD1871's analog Σ-Δ modulator section comprises a second order multibit implementation using Analog Device's proprietary technology for best performance. As shown in Figure 9, the two analog integrator blocks are followed by a Flash ADC section that generates the multibit samples. The output of the Flash ADC, which is thermometer encoded, is decoded to binary for output to the filter sections and is scrambled for feedback to the two integrator stages.

The modulator is optimized for operation at a sampling rate of 6.144 MHz (which is $128 \times f_S$ at 48 kHz sampling and $64 \times f_S$ at 96 kHz sampling). The modulator clock control (AMC Bit in Control Register I) is used to select the modulator clock (MODCLK) as a ratio from the IMCLK. The modulator clock divider options are /2 (default) for 48 kHz operation and /4 for 96 kHz operation. When operating with an IMCLK of 12.288 MHz, the default divider setting (/2) gives a modulator clock of 6.144 MHz. When operating with an IMCLK of 24.576 MHz, the alternate divider setting (/4) gives a modulator clock of 6.144 MHz (see Figure 8).

If it is required to operate the device at a different output sample rate than those detailed above, perhaps 44.1 kHz or 88.2 kHz, the decimation filter cutoff characteristics can then be determined from the normalized frequency response plot shown in TPC 6.

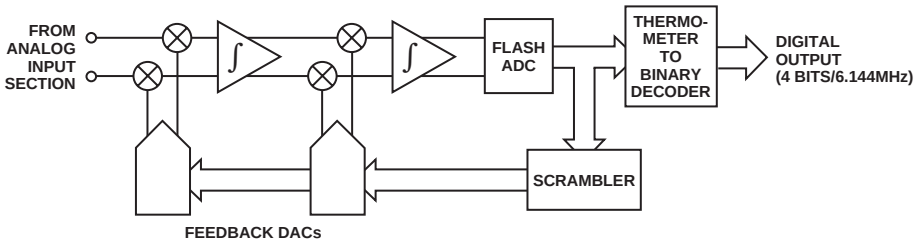


Figure 9. Modulator Block Diagram

Digital Decimating Filters

The filtering and decimation of the AD1871's modulator data stream is implemented in an embedded DSP engine. The first stage of filtering is the sinc filtering, which has selectable decimation (selected by the modulator clock control bit (AMC, see Modulator section). The default decimation in the sinc stage provides a sample rate reduction of 16; this corresponds with a MODCLK rate of $128 \times f_S$. The alternate setting of the AMC Bit gives a sinc decimation factor of 8 that corresponds with a MODCLK rate of $64 \times f_S$. The output of the sinc decimator stage is at a rate of $8 \times f_S$.

The filter engine implements two half-band FIR filter sections and a sinc compensation stage that together give a further decimation factor of 8. Please refer to TPCs 1 through 4 for details on the responses of the sinc and FIR filter sections. TPC 5 gives the composite response of the sinc and FIR filters.

High-Pass Filter

The AD1871 features an optional high-pass filter section that provides the ability of rejecting dc from the output data stream. The high-pass filter is enabled by setting Bit 8 (HPE) of Control Register I to 1. Please refer to TPC 7 and TPC 8 for details of the high-pass filter characteristics.

ADC Coding

The ADC's output data stream is in a two's complement encoded format. The word width can be selected from 16 bits, 20 bits, or 24 bits (see Table VI and Table VII). The coding scheme is detailed in Table I.

Table I. ADC Coding

Code	Level
011111.....1111	+Full Scale
000000.....0000	0 (Ref Level)
100000.....0001	–Full Scale

Analog Input Section

The analog input section comprises a differential PGA stage. It can also be configured for single-ended inputs, allowing two such inputs to be selected via a multiplex switch. The PGA has five gain settings (see Table V) ranging from 0 dB to 12 dB in 3 dB steps.

In Differential Mode, the VINxP and VINxN input pins are connected to a pair of inverting amplifiers whose outputs are connected to the CAPxN and CAPxP pins, respectively. (See Figure 10.)

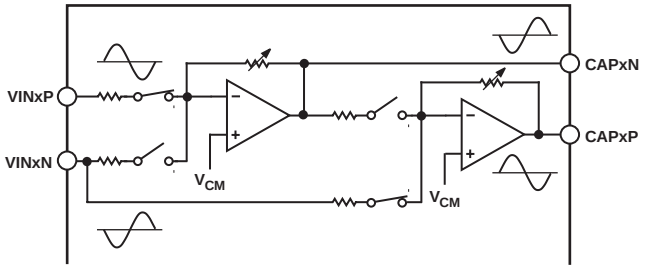


Figure 10. Differential Analog Input

In Single-Ended Mode, either VINxP or VINxN can be selected as the input. The pair of input inverting amplifiers is reconfigured as a single-ended-to-differential conversion stage. Again the outputs of the differential section are connected to Pins CAPxP and CAPxN (see Figure 11).

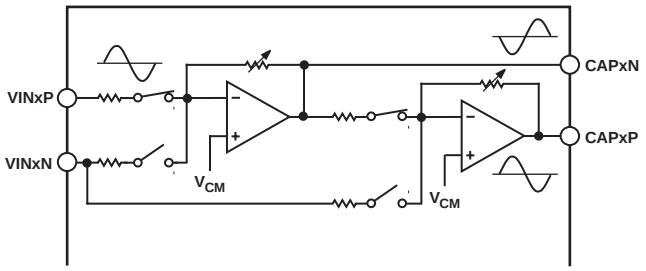


Figure 11. Single-Ended Analog Input

The analog input section is enabled (powered ON) by default on reset. If it is required to bypass the analog input section by using the modulator input pins (CAPxP and CAPxN) directly, then the analog input section must be powered down by setting Bits MER and MEL in Control Register III.

Serial Data Interface

The AD1871's serial data interface consists of three pins (LRCLK, BCLK, and SDATA). LRCLK is the framing signal for left and right channel samples and its frequency is equal to the sampling frequency (f_S). BCLK is the serial clock used to clock the data samples from the AD1871 and its frequency is equal to $64 \times f_S$ (giving 32 BCLK periods for each of the left and right channels). SDATA outputs the left and right channel sample data coincident with the falling edge of BCLK.

The serial data interface supports all the popular audio interface standards, such as I^2S, left-justified (LJ), and right-justified (RJ), as well as the serial interfaces of modern DSPs. The Interface Mode is selected by programming the Bits DF1–DF0 of Control Register II (see Tables VI and VIII).

The data sample width can be selected from 16, 20, or 24 bits by programming Bits WW1–WW0 of Control Register II (see Tables VI and VII).

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