



40-Channel, 5V Single Supply, 12-Bit, Voltage-Output DAC

Preliminary Technical Data

AD5381

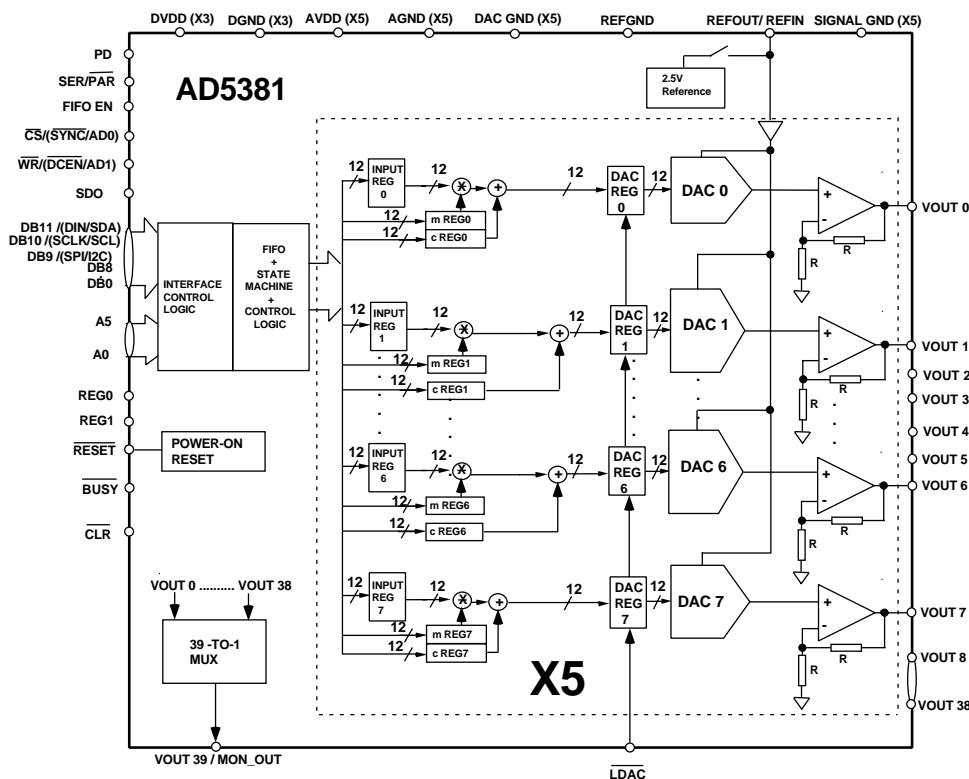
FEATURES

- 40-Channel, 12-Bit, Voltage Out DAC
 - ±1 LSB max INL, ±1 LSB max DNL
 - Package Type: 100-lead LQFP (14mm x 14mm)
 - User Interfaces:
 - Parallel
 - Serial: SPI, QSPI, Microwire and DSP-/Microcontroller compatible
 - I2C Compatible Interface
 - On-chip Output Amplifier with Rail to Rail Operation
 - Settling Time Boost Mode
 - System Calibration Function allowing User Programmable Offset and Gain Adjust
 - On-chip 1.25/2.5V, 10ppm/°C Reference
 - Clear Function to User Programmable Code
 - Simultaneous Update of DAC Outputs (LDAC Pin)
 - Power-On-Reset
- ### APPLICATIONS
- Variable Optical Attenuators (VOA)
 - Level Setting
 - Optical Microelectromechanical Systems (MEMs)
 - Control Systems

GENERAL DESCRIPTION

The AD5381 is a complete single supply, 40-channel, 12-bit, voltage out DAC available in a 100-lead LQFP package. All 40-channels have an on-chip output amplifier with rail-to-rail operation. The AD5381 includes an internal 1.25/2.5V, 10ppm/°C reference, an on-chip channel monitor function that multiplexes the analog outputs to a common MON_OUT pin for external monitoring and an output amplifier boost mode that allows the amplifier settling time to be optimized. The AD5381 contains a double buffered parallel interface featuring a WR pulse width of 20ns, a serial interface compatible with SPI™, QSPI™, MICROWIRE™ and DSP interface standards with interface speeds in excess of 30MHz and an I2C compatible interface supporting 400kHz data transfer rate. An input register followed by a DAC register provides double buffering allowing the DAC outputs to be updated independently or simultaneously using the LDAC input. Each channel has a programmable gain and offset adjust register allowing the user to fully calibrate any DAC Channel. Power consumption is typically 0.3mA/channel.

FUNCTIONAL BLOCK DIAGRAM



*Protected by U.S. Patent Nos. 5,969,657; other patents pending.

SPI and QSPI are Trademarks of Motorola, Inc.

MICROWIRE is a Trademark of National Semiconductor Corporation.

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PRELIMINARY TECHNICAL DATA

AD5381—SPECIFICATIONS ($A_{V_{DD}} = 4.5V$ to $5.5V$; $DV_{DD} = 2.7V$ to $5.5V$, $AGND = DGND = 0V$; $C_L = 200$ pF to $AGND$; $R_L = 5k\Omega$; External $REFIN = 2.5V$; All specifications T_{MIN} to T_{MAX} unless otherwise noted.)

Parameter	AD5381 ¹	Units	Test Conditions/Comments
ACCURACY			
Resolution	12	Bits	Guaranteed Monotonic Over Temp Measured at code 32 in the linear region
Relative Accuracy ³	±1	LSB max	
Differential Nonlinearity	±1	LSB max	
Zero-Scale Error	±10	mV max	
Offset Error	±10	mV max	
Offset Error TC	±5	uV/°C typ	
Gain Error	±0.02	% FSR max	
Gain Temperature Coefficient ²	20	ppm FSR/°C typ	
DC Crosstalk ²	0.5	LSB max	
REFERENCE INPUT/OUTPUT			
REFERENCE INPUT²			±1% for Specified Performance Typically 100 MΩ Typically ±30 nA V min/max
Reference Input Voltage	2.5	V	
DC Input Impedance	1	MΩ min	
Input Current	±10	μA max	
Reference Range	1V to $V_{DD}/2$		
REFERENCE OUTPUT⁴			At Ambient. CR10=1 At Ambient. CR10=0
Output Voltage	2.495/2.505	V min/max	
Reference TC	1.248/1.252	V min/max	
Reference TC	±10	ppm/°C typ	
OUTPUT CHARACTERISTICS²			
Output Voltage Range ³	0/ $A_{V_{DD}}$	V min/max	
Short Circuit Current	40	mA max	
Load Current	±1	mA max	
Capacitive Load Stability			
$R_L = \infty$	200	pF max	
$R_L = 5k\Omega$	TBD	pF max	
DC Output Impedance	0.5	Ω max	
MONITOR PIN			
Output Impedance	500	Ω typ	
Tristate Leakage Current	100	nA typ	
LOGIC INPUTS (EXCEPT SDA/SCL)²			$DV_{DD} = 2.7V$ to $5.5V$
V_{IH} , Input High Voltage	2	V min	Total for All Pins. $T_A = T_{MIN}$ to T_{MAX} SMBus-Compatible at $V_{DD} < 3.6V$ SMBus-Compatible at $V_{DD} < 3.6V$ Input filtering suppresses noise spikes of less than 50 ns.
V_{IL} , Input Low Voltage	0.8	V max	
Input Current	±10	μA max	
Pin Capacitance	10	pF max	
LOGIC INPUTS (SCL, SDA ONLY)			
V_{IH} , Input High Voltage	0.7 DV_{DD}	V min	
V_{IL} , Input Low Voltage	0.3 DV_{DD}	V max	
I_{IN} , Input Leakage Current	±1	μA	
V_{HYST} , Input Hysteresis	0.05 DV_{DD}	V	
C_{IN} , Input Capacitance	8	pF	
Glitch Rejection	50	ns	
LOGIC OUTPUTS (\overline{BUSY}, SDO)²			
V_{OL} , Output Low Voltage	0.4	V max	$DV_{DD} = 5V \pm 10\%$, Sinking 200μA $DV_{DD} = 5V \pm 10\%$, Sourcing 200μA $DV_{DD} = 2.7V$ to $3.6V$, Sinking 200μA $DV_{DD} = 2.7V$ to $3.6V$, Sourcing 200μA SDO Only SDO Only $I_{SINK} = 3mA$ $I_{SINK} = 6mA$
V_{OH} , Output High Voltage	$DV_{DD} - 1$	V min	
V_{OL} , Output Low Voltage	0.4	V max	
V_{OH} , Output High Voltage	$DV_{DD} - 0.5$	V min	
High Impedance Leakage Current	±1	μA max	
High Impedance Output Capacitance	5	pF typ	
LOGIC OUTPUT (SDA)²			
V_{OL} , Output Low Voltage	0.4	V max	
	0.6	V max	
Three-State Leakage Current	±1	μA	
Three-State Output Capacitance	8	pF	

AD5381—SPECIFICATIONS

($V_{DD} = 4.5V$ to $5.5V$; $DV_{DD} = 2.7V$ to $5.5V$, $AGND = DGND = 0V$;
 $C_L = 200$ pF to $AGND$; $R_L = 5k\Omega$; External $REFIN = 2.5V$;
 All specifications T_{MIN} to T_{MAX} unless otherwise noted.)

POWER REQUIREMENTS			
AV_{DD}	4.5/5.5	V min/max	
DV_{DD}	2.7/5.5	V min/max	
Power Supply Sensitivity ² Δ Mid Scale/ ΔAV_{DD}	-85	dB typ	
AI_{DD}	0.5	mA/Channelmax	Outputs Unloaded. Boost Off. XXmA typ
AI_{DD}	0.57	mA/Channelmax	Outputs Unloaded. Boost On. XXmA typ
DI_{DD}	5	mA max	$V_{IH} = DV_{DD}$, $V_{IL} = DGND$. XXmA typ
AI_{DD} (Power Down)	5	uA max	
DI_{DD} (Power Down)	5	uA max	
Power Dissipation	125	mW max	Outputs Unloaded.

NOTES

¹Temperature range for All Versions: $-40^{\circ}C$ to $+85^{\circ}C$

²Guaranteed by characterization. Not production tested.

³Accuracy guaranteed from $V_{out} = 10mV$ to $AV_{DD} - 50mV$

⁴Programmable to either 1.25V typ or 2.5V typ via CR10 in the AD5381 control register.

Specifications subject to change without notice.

AC CHARACTERISTICS¹ ($V_{DD} = 4.5V$ to $5.5V$; $DV_{DD} = 2.7V$ to $5.5V$; $AGND = DGND = 0V$; $C_L = 5k\Omega$ and 200 pF to $AGND$)

Parameter	All	Units	Test Conditions/Comments
DYNAMIC PERFORMANCE			
Output Voltage Settling Time ²	6	μs typ	Boost Mode Off, CR9=0
	8	μs max	1/4 Scale to 3/4 Scale Change settling to $\pm 1LSB$.
Output Voltage Settling Time ²	2	μs typ	Boost Mode On, CR9=1
	4	μs max	1/4 Scale to 3/4 Scale Change settling to $\pm 1LSB$.
Slew Rate ²	0.7	V/ μs typ	Boost Mode Off, CR9=0
	1.5	V/ μs typ	Boost Mode On, CR9=1
Digital-to-Analog Glitch Energy	12	nV-s typ	
Glitch Impulse Peak Amplitude	5	mV max	
Channel-to-Channel Isolation	100	dB typ	See Terminology
DAC-to-DAC Crosstalk	10	nV-s typ	See Terminology
Digital Crosstalk	10	nV-s typ	
Digital Feedthrough	1	nV-s typ	
Output Noise 0.1 to 10Hz	8	uV p-p	Effect of Input Bus Activity on DAC Output Under Test
Output Noise Spectral Density			
@ 1 kHz	150	nV/(Hz) ^{1/2} typ	
@ 10 kHz	100	nV/(Hz) ^{1/2} typ	

¹Guaranteed by design and characterization, not production tested.

²The Settling Time and Slew Rate can be programmed via the Current Boost Control bit (CR9) in the AD5381 Control Register. Specifications subject to change without notice.

PRELIMINARY TECHNICAL DATA

TIMING CHARACTERISTICS

($DV_{DD}= 2.7V$ to $5.5V$; $AV_{DD}=+4.5V$ to $+5.5V$; $AGND= DGND = 0 V$;)
 All specifications T_{MIN} to T_{MAX} unless otherwise noted.)

SERIAL INTERFACE

Parameter ^{1,2,3}	Limit at T_{MIN} , T_{MAX}	Units	Description
t_1	33	ns min	SCLK Cycle Time
t_2	13	ns min	SCLK High Time
t_3	13	ns min	SCLK Low Time
t_4	13	ns min	\overline{SYNC} Falling Edge to SCLK Falling Edge Setup Time
t_5^4	13	ns min	24th SCLK Falling Edge to \overline{SYNC} Falling Edge
t_6^4	33	ns min	Minimum \overline{SYNC} Low Time
t_7	10	ns min	Minimum \overline{SYNC} High Time
t_8	5	ns min	Data Setup Time
t_9	4.5	ns min	Data Hold Time
$t_{10}^{4,5}$	30	ns max	24th SCLK Falling Edge to \overline{BUSY} Falling Edge
t_{11}	900	ns typ	\overline{BUSY} Pulse Width Low (Single Channel Update)
t_{12}^4	20	ns min	24th SCLK Falling Edge to \overline{LDAC} Falling Edge
t_{13}	20	ns min	\overline{LDAC} Pulse Width Low
t_{14}	100	ns max	\overline{BUSY} Rising Edge to DAC Output Response Time
t_{15}	0	ns min	\overline{BUSY} Rising Edge to \overline{LDAC} Falling Edge
t_{16}	100	ns min	\overline{LDAC} Falling Edge to DAC Output Response Time
t_{17}	6	μs typ	DAC Output Settling Time, Boost Mode off.
t_{18}	20	ns min	\overline{CLR} Pulse Width Low
t_{19}	12	μs max	\overline{CLR} Pulse Activation Time
$t_{20}^{6,7}$	20	ns max	SCLK Rising Edge to SDO Valid
t_{21}^7	5	ns min	SCLK Falling Edge to \overline{SYNC} Rising Edge
t_{22}^7	8	ns min	\overline{SYNC} Rising Edge to SCLK Rising Edge
t_{23}^7	20	ns min	\overline{SYNC} Rising Edge to \overline{LDAC} Falling Edge

NOTES

¹Guaranteed by design and characterization, not production tested.

²All input signals are specified with $t_r = t_f = 5$ ns (10% to 90% of V_{CC}) and timed from a voltage level of 1.2 V.

³See Figures 3 and 4

⁴Stand-Alone Mode only.

⁵This is measured with the load circuit of Figure 1a.

⁶This is measured with the load circuit of Figure 1b.

⁷Daisy-Chain Mode only.

Specifications subject to change without notice.

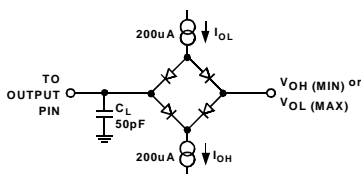


Figure 1b. Load Circuit for SDO Timing Diagram (Serial Interface, Daisy-Chain mode)

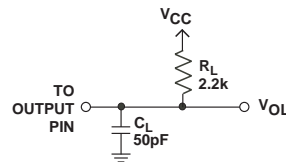
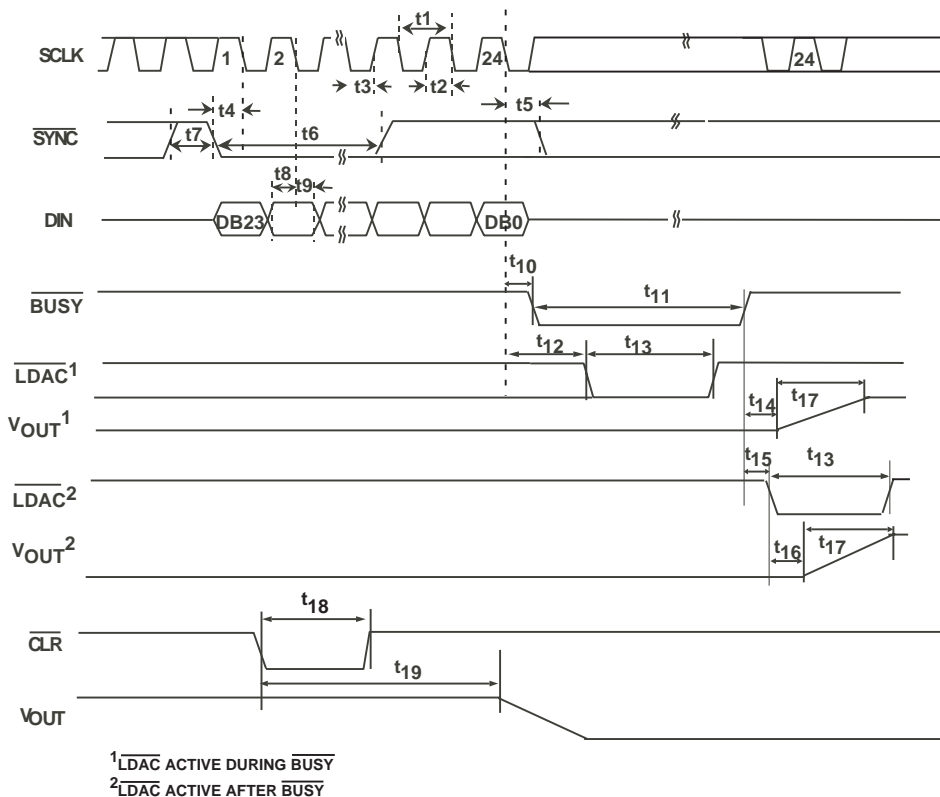


Figure 1a Load Circuit for $\overline{\text{BUSY}}$ Timing Diagram



¹LDAC ACTIVE DURING $\overline{\text{BUSY}}$
²LDAC ACTIVE AFTER $\overline{\text{BUSY}}$

Figure 3. Serial Interface Timing Diagram (Stand-Alone mode)

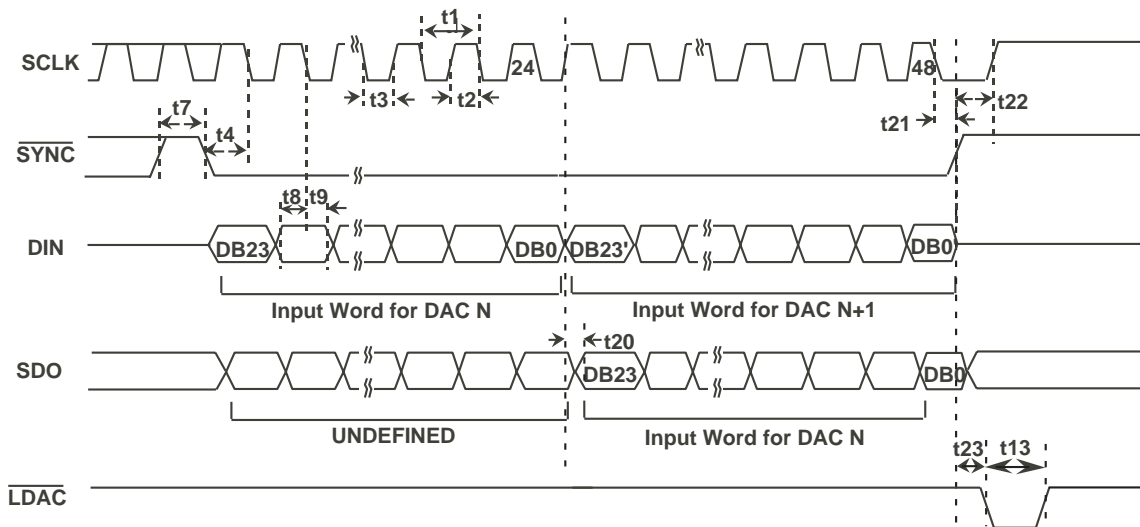


Figure 4. Serial Interface Timing Diagram (Daisy-Chain mode)

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TIMING CHARACTERISTICS

($V_{DD}= 2.7V$ to $5.5V$; $AV_{DD}=+4.5V$ to $+5.5V$; $AGND= DGND = 0 V$;)
 All specifications T_{MIN} to T_{MAX} unless otherwise noted.)

I²C SERIAL INTERFACE

Parameter ^{1,2}	Limit at T_{MIN}, T_{MAX}	Units	Description
F_{SCL}	400	kHz max	SCL Clock Frequency
t_1	2.5	μs min	SCL Cycle Time
t_2	0.6	μs min	t_{HIGH} , SCL High Time
t_3	1.3	μs min	t_{LOW} , SCL Low Time
t_4	0.6	μs min	$t_{HD,STA}$, Start/Repeated Start Condition Hold Time
t_5	100	ns min	$t_{SU,DAT}$, Data Setup Time
t_6^3	0.9	μs max	$t_{HD,DAT}$, Data Hold Time
t_7	0	μs min	$t_{HD,DAT}$, Data Hold Time
t_8	0.6	μs min	$t_{SU,STA}$, Setup Time for Repeated Start
t_9	0.6	μs min	$t_{SU,STO}$, Stop Condition Setup Time
t_{10}	1.3	μs min	t_{BUF} , Bus Free Time Between a STOP and a START Condition
t_{11}	300	ns max	t_R , Rise Time of SCL and SDA when Receiving
	0	ns min	t_R , Rise Time of SCL and SDA when Receiving (CMOS-Com patible)
	300	ns max	t_F , Fall Time of SDA when Transmitting
	0	ns min	t_F , Fall Time of SDA when Receiving (CMOS-Compatible)
	300	ns max	t_F , Fall Time of SCL and SDA when Receiving
	$20 + 0.1C_B^3$	ns min	t_F , Fall Time of SCL and SDA when Transmitting
C_B	400	pF max	Capacitive Load for Each Bus Line

NOTES

¹Guaranteed by design and characterization, not production tested.

²See Figures 5

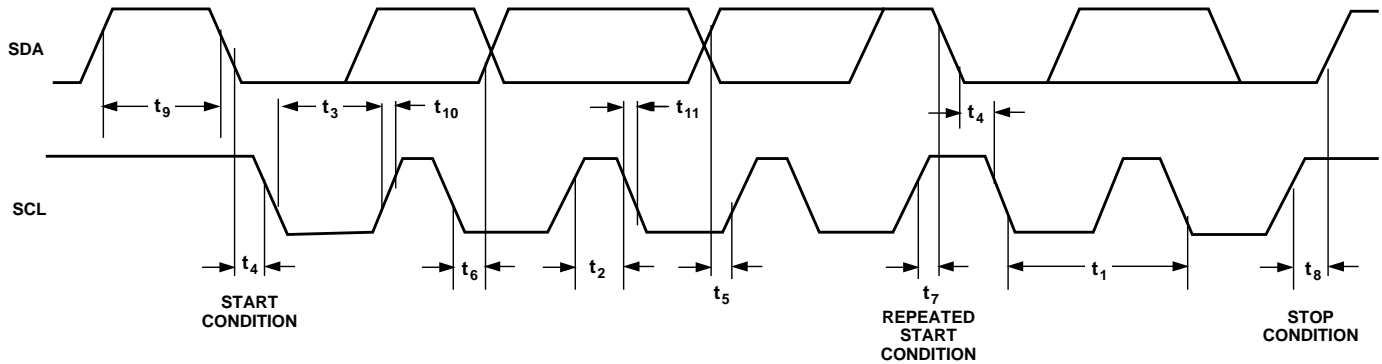


Figure 5. I²C Compatible Serial Interface Timing Diagram

TIMING CHARACTERISTICS ($DV_{DD} = 2.7\text{ V to }+5.5\text{V}$; $AV_{DD} = 5\text{ V} \pm 10\%$; $AGND = DGND = 0\text{ V}$;
All specifications T_{MIN} to T_{MAX} unless otherwise noted.)

PARALLEL INTERFACE

Parameter ^{1,2,3}	Limit at T_{MIN} , T_{MAX}	Units	Description
t_0	4.5	ns min	REG0,REG1,Address to \overline{WR} Rising Edge Setup Time
t_1	4.5	ns min	REG0,REG1, Address to \overline{WR} Rising Edge Hold Time
t_2	20	ns min	\overline{CS} Pulse Width Low
t_3	20	ns min	\overline{WR} Pulse Width Low
t_4	0	ns min	\overline{CS} to \overline{WR} Falling Edge Setup Time
t_5	0	ns min	\overline{WR} to \overline{CS} Rising Edge Hold Time
t_6	4.5	ns min	Data to \overline{WR} Rising Edge Setup Time
t_7	4.5	ns min	Data to \overline{WR} Rising Edge Hold Time
t_8	20	ns min	\overline{WR} Pulse Width High
t_9 ⁴	430	ns min	Minimum \overline{WR} Cycle Time (Single Channel Write)
t_{10} ⁴	30	ns max	\overline{WR} Rising Edge to \overline{BUSY} Falling Edge
t_{11} ^{4,5}	400	ns max	\overline{BUSY} Pulse Width Low (Single Channel Update)
t_{12} ⁴	30	ns min	\overline{WR} Rising Edge to \overline{LDAC} Falling Edge
t_{13}	20	ns min	\overline{LDAC} Pulse Width Low
t_{14} ⁴	100	ns max	\overline{BUSY} Rising Edge to DAC Output Response Time
t_{15}	20	ns min	\overline{LDAC} Rising Edge to \overline{WR} Rising Edge
t_{16}	0	ns min	\overline{BUSY} Rising Edge to \overline{LDAC} Falling Edge
t_{17} ⁴	100	ns min	\overline{LDAC} Falling Edge to DAC Output Response Time
t_{18}	6	$\mu\text{s typ}$	DAC Output Settling Time, Boost mode off.
t_{19}	20	ns min	\overline{CLR} Pulse Width Low
t_{20}	12	$\mu\text{s max}$	\overline{CLR} Pulse Activation Time

NOTES

¹Guaranteed by design and characterization, not production tested.

²All input signals are specified with $t_r = t_f = 5\text{ ns}$ (10% to 90% of V_{CC}) and timed from a voltage level of 1.2 V.

³See Timing Diagram in Figure 6.

⁴See Table XXX.

⁵This is measured with the load circuit of Figure 1a.

Specifications subject to change without notice.

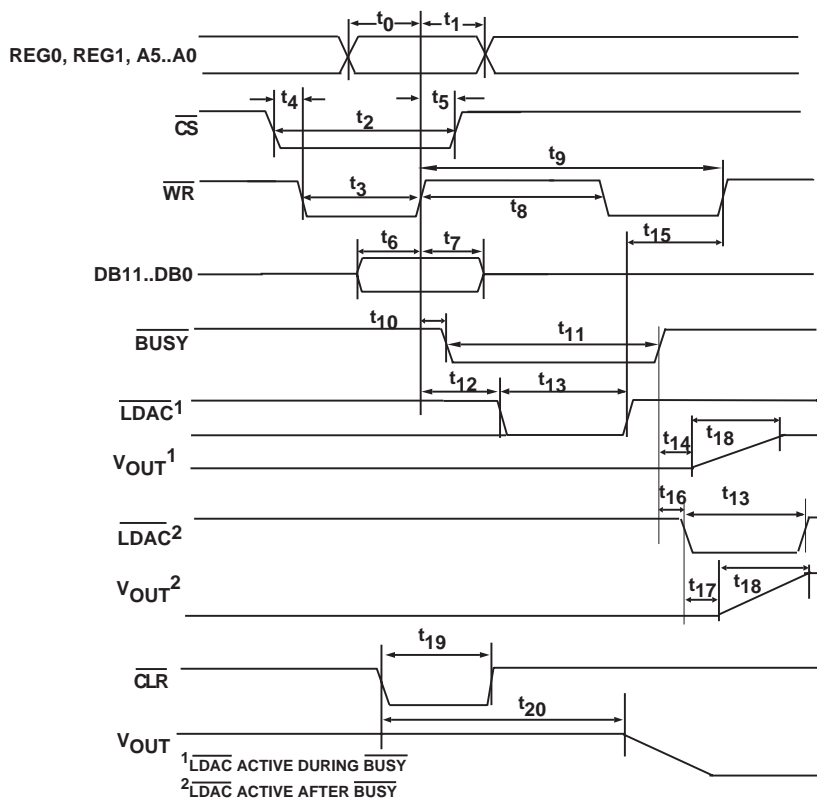


Figure 6. Parallel Interface Timing Diagram

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ABSOLUTE MAXIMUM RATINGS^{1,2}

(T_A = +25°C unless otherwise noted)

AV _{DD} to AGND.....	-0.3 V to +7 V
DV _{DD} to DGND.....	-0.3 V to +7 V
Digital Inputs to DGND.....	-0.3 V to DV _{DD} + 0.3 V
SDA/SCL to DGND.....	-0.3 V to + 7 V
Digital Outputs to DGND.....	-0.3 V to DV _{DD} + 0.3 V
REFIN/REFOUT to AGND.....	-0.3 V to AV _{DD} + 0.3 V
AGND to DGND.....	-0.3 V to +0.3 V
VOU0-39 to AGND.....	- 0.3 V to AV _{DD} + 0.3 V
Analog Inputs to AGND.....	- 0.3 V to AV _{DD} + 0.3 V

Operating Temperature Range	
Commercial (B Version).....	-40°C to +85°C
Storage Temperature Range.....	-65°C to +150°C
Junction Temperature	
(T _{Jmax}).....	+150°C
100-lead LQFP Package,	
θ _{JA} Thermal Impedance.....	TBD°C/W
Reflow Soldering	
Peak Temperature.....	230°C

NOTES:

¹Stresses above those listed under “Absolute Maximum Ratings” may cause permanent damage to the device. This is a stress rating only, and functional operation of the device at these or any other conditions above those listed in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

²Transient currents of up to 100mA will not cause SCR latch-up

ORDERING GUIDE

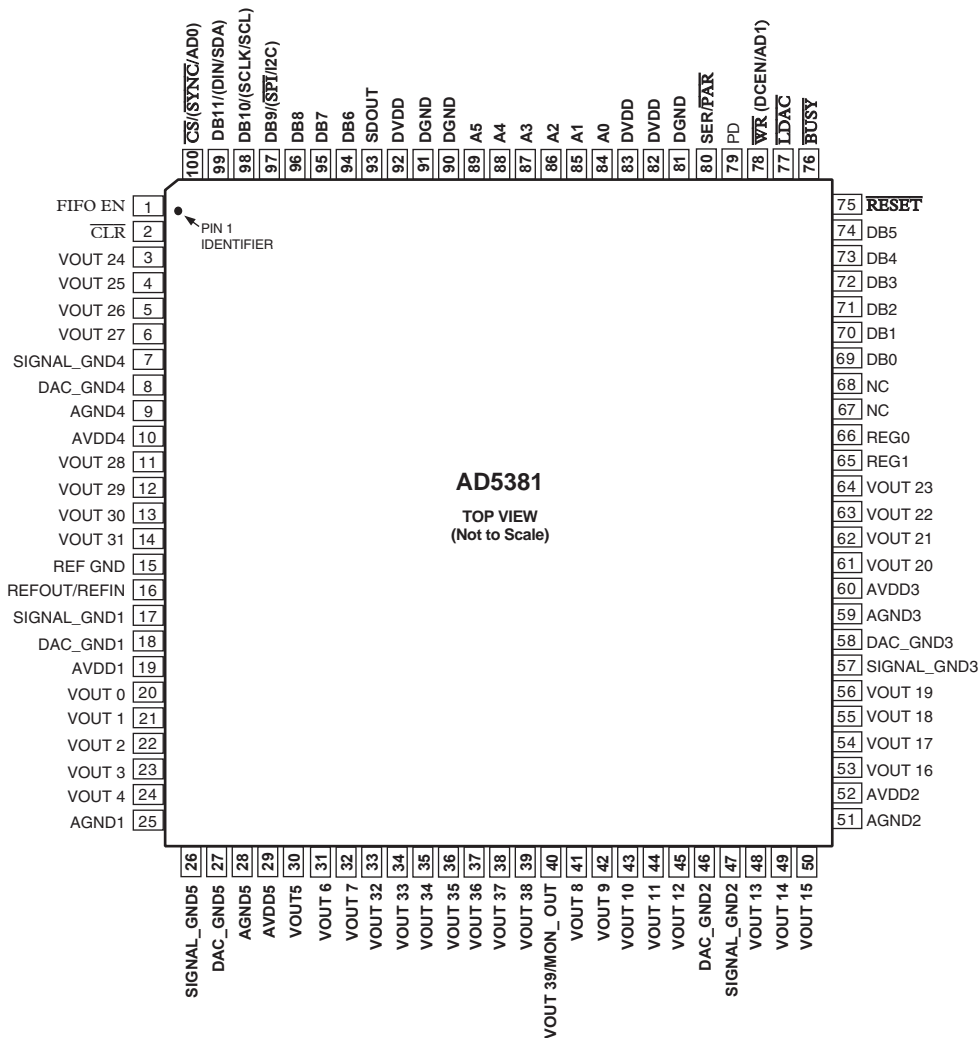
Model Option	Resolution	Output Channels	Linearity Error (LSBs)	Package	Package Description
AD5381BST	12-Bits	40	± 1	100-lead LQFP	ST-100

CAUTION

ESD (electrostatic discharge) sensitive device. Electrostatic charges as high as 4000 V readily accumulate on the human body and test equipment and can discharge without detection. Although the AD5381 features proprietary ESD protection circuitry, permanent damage may occur on devices subjected to high energy electrostatic discharges. Therefore, proper ESD precautions are recommended to avoid performance degradation or loss of functionality.



PIN CONFIGURATIONS
AD5381 (40-CHANNEL, 12-BIT)



AD5381 PIN FUNCTION DESCRIPTIONS

Mnemonic	Function
VOUTX	Buffered analog outputs for channel X. Each analog output is driven by a rail to rail output amplifier operating at a gain of 2. Each output is capable of driving an output load of 5k to ground. Typical output impedance is 0.5 ohms.
SIGNAL_GND(1-5)	Analog ground reference points for each group of 8 output channels. All signal_gnd pins are tied together internally and should be connected to AGND plane as close as possible to the AD5381.
DAC-GND (1-5)	Each group of 8 channels contains a DAC_GND pin. This is the ground reference point for the internal 12-bit DACs. These pins should be connected to the AGND plane.
AGND (1-5)	Analog Ground reference point. Each group of 8 channels contains an AGND pin. All AGND pins should be connected externally to the AGND plane.
AVDD (1-5)	Analog Supply pins. Each group of 8 channels has a separate AVDD pin. These pins should be decoupled with 0.1uF ceramic capacitors and 10uF tantalum capacitors. Operating range is 5V +/-10%
DGND	Ground for all digital circuitry.
DVDD	Logic Power Supply; Guaranteed operating range is 2.7 V to 5.5 V. Recommended that

AD5381

	these pins be decoupled with 0.1uF ceramic and 10uF tantalum capacitors to DGND.
REF-GND	Ground Reference point for the internal reference.
REFOUT/REFIN	The AD5381 contains a common REFOUT/REF IN pin. When the internal reference is selected this pin is the reference output. If the application necessitates the use of an external reference, it can be applied to this pin and the internal reference disabled via the control register. The default for this pin is a reference input.
VOUT39/MON_OUT	This pin has a dual function, it acts as a buffered output for channel 39 in default mode but when the monitor function is enabled this output acts as the output of a 39-to-1 channel multiplexer which can be programmed to multiplex one of channels 0 to 38 to the MON_OUT pin. The MON_OUT pins output impedance is typically 500 ohms and is intended to drive a high input impedance like that exhibited by SAR ADC inputs.
SER/ $\overline{\text{PAR}}$.	Interface Select Input. This pin allows the user to select whether the serial or parallel interface will be used. If it is tied high the serial interface mode is selected and pin 97 ($\overline{\text{SPI}}$ /I2C) is used to determine if the interface mode is SPI or I2C. Parallel interface mode is selected when SER/ $\overline{\text{PAR}}$ is low.
$\overline{\text{CS}}$ / $\overline{(\text{SYN}\overline{\text{C}}/\text{AD0})}$	In parallel interface mode this pin acts as Chip Select Input (level sensitive, active low). When low the AD538X device is selected. Serial Interface Mode: This is the Frame Synchronisation input signal for the serial interface. When taken low the internal counter is enabled to count the required number of clocks before the addressed register is updated. I2C Mode: This pin acts as a hardware address pin used in conjunction with AD1 to determine the software address for the device on the I2C bus.
$\overline{\text{WR}}$ / $\overline{(\text{DCEN}/\text{AD1})}$	Multi Function pin. In parallel interface mode acts as Write enable and in serial interface mode acts as a daisy chain enable in SPI mode and as a hardware address pin in I2C mode. Parallel Interface Write Input (edge sensitive). The rising edge of $\overline{\text{WR}}$ is used in conjunction with $\overline{\text{CS}}$ low and the address bus inputs to write to the selected device registers. Serial Interface: Daisy-Chain Select Input (level sensitive, active high). When high this signal is used in conjunction with SER/ $\overline{\text{PAR}}$ high to enable SPI serial interface daisy-chain mode. I2C Mode: This pin acts as a hardware address pin used in conjunction with AD0 to determine the software address for this device on the I2C bus.
DB0-DB11	Parallel Data Bus. DB11 is the MSB and DB0 is the LSB of the input data word on the AD5381
A0-A5	Parallel Address Inputs. A5 to A0 are decoded to address one of the 40 input channels on the AD5381. Used in conjunction with the REG1 and REG0 pins to determine the destination register for the input data.
REG1,REG0	REG1 and REG0 are used in decoding the destination registers for the input data. REG1 and REG0 are decoded to address the input data register, offset register or gain register for the selected channel and also are used to decide the special function registers.
SDOUT	Serial Data Output. Tristatable CMOS output. SDO can be used for daisy-chaining a number of devices together. Data is clocked out on SDO on the rising edge of SCLK and is valid on the falling edge of SCLK.
$\overline{\text{BUSY}}$	Digital CMOS Output. $\overline{\text{BUSY}}$ goes low during internal calculations of x2. During this time the user can continue writing new data to further x1, c and m registers (these are stored in a FIFO) but no further updates to the DAC registers and DAC outputs can take place. If $\overline{\text{LDAC}}$ is taken low while $\overline{\text{BUSY}}$ is low this event is stored. $\overline{\text{BUSY}}$ also goes low during power-on-reset or when the $\overline{\text{RESET}}$ pin is low. During this time the interface is disabled and any events on $\overline{\text{LDAC}}$ are ignored.
$\overline{\text{LDAC}}$	Load DAC Logic Input (active low). If $\overline{\text{LDAC}}$ is taken low while $\overline{\text{BUSY}}$ is inactive (high) the contents of the input registers are transferred to the DAC registers and the DAC outputs are updated. If $\overline{\text{LDAC}}$ is taken low while $\overline{\text{BUSY}}$ is active and internal calculations are taking place, the $\overline{\text{LDAC}}$ event is stored and the DAC registers are updated when $\overline{\text{BUSY}}$ goes inactive. However any events on $\overline{\text{LDAC}}$ during power-on-reset or $\overline{\text{RESET}}$ are ignored.
$\overline{\text{CLR}}$	Asynchronous Clear Input (level sensitive, active low). While $\overline{\text{CLR}}$ is low all $\overline{\text{LDAC}}$ pulses are ignored. When $\overline{\text{CLR}}$ is activated all channels are updated with the data contained in the $\overline{\text{CLR}}$ code register. $\overline{\text{BUSY}}$ is low for a duration of 12us while all channels are being updated with the $\overline{\text{CLR}}$ code.
$\overline{\text{RESET}}$	Asynchronous Digital Reset Input (falling edge sensitive). The function of this pin is equivalent to that of the Power-On-Reset generator. When this pin is taken low, the state-machine initiates a reset sequence to digitally reset x1, m, c, and x2 registers to their default

	power-on values. This sequence takes 300us (typ). The falling edge of \overline{RESET} initiates the RESET process and \overline{BUSY} goes low for the duration returning high when \overline{RESET} is complete. While \overline{BUSY} is low all interfaces are disabled and all LDAC pulses are ignored. When \overline{BUSY} returns high the part resumes normal operation and the status of the RESET pin is ignored till the next falling edge is detected.
PD	Power Down (level sensitive active high). Used to place the device in low power mode where the device consumes less than 5uA. In power pown mode all internal analog circuitry is placed in low power mode, the analog output will be configured as high impedance outputs or will provide a 100k load to ground depending on how the power down mode is configured. The serial interface remains active during power down.
FIFO_EN	FIFO Enable (level sensitive active high). When connected to DVCC the internal FIFO is enabled allowing the user to write to the device at full speed. FIFO is only available in parallel interface mode. The status of the FIFO_EN pin is sampled on power-up, and also following a CLEAR or RESET to determine if the FIFO is enabled. In either serial or I2C interface modes the FIFO_EN pin should be tied low.
NC	No Connect. The user is advised not to connect any signals to these pins.
DB9 ($\overline{SPI}/I2C$)	Multi-function input pin. In parallel interface mode this pin acts as DB9 of the parallel input data word. In serial interface mode this pin acts as serial interface mode select. When serial interface mode is selected ($\overline{SER}/\overline{PAR} = 1$) and this input is low SPI Mode is selected. In this mode DB10 is the serial clock (SCLK) input and DB113 is the serial data (DIN) input. When serial interface mode is selected ($\overline{SER}/\overline{PAR} = 1$) and this input is high I2C Mode is selected. In this mode DB10 is the serial clock (SCL) input and DB11 is the serial data (SDA) input.
DB10 (SCLK/SCL)	Multi-function input pin. In parallel interface mode this pin acts as DB10 of the parallel input data word. In serial interface mode this pin acts as a serial clock input. SPI Mode: In SPI mode data is clocked into the shift register on the falling edge of SCLK. This operates at clock speeds up to 50 MHz. I2C Mode: In I2C mode this pin performs the SCL function, clocking data into the device. Data transfer rate in I2C mode is compatible with both 100kHz and 400kHz operating modes.
DB11/(DIN/SDA)	Multi-function data input pin. In parallel interface mode this pin acts as DB11 (MSB) of the parallel input data word on the AD5381. Serial Interface Mode: In serial interface mode this pin acts as the serial data input. Data must be valid on the falling edge of SCLK. I2C Mode: In I2C mode this pin is the serial Data pin (SDA) operating as an open drain input/output.

AD5381

TERMINOLOGY**Relative Accuracy**

Relative accuracy or endpoint linearity is a measure of the maximum deviation from a straight line passing through the endpoints of the DAC transfer function. It is measured after adjusting for zero-scale error and full-scale error and is expressed in Least Significant Bits.

Differential Nonlinearity

Differential nonlinearity is the difference between the measured change and the ideal 1 LSB change between any two adjacent codes. A specified differential nonlinearity of 1 LSB maximum ensures monotonicity.

Zero-Scale Error

Zero-scale error is the error in the DAC output voltage when all 0s are loaded into the DAC register.

Ideally, with all 0s loaded to the DAC and $m = \text{all } 1\text{s}$, $c = 2^{n-1}$:

$$V_{OUT}(\text{Zero-Scale}) = 0V$$

Zero-scale error is a measure of the difference between V_{OUT} (actual) and V_{OUT} (ideal) expressed in mV. It is mainly due to offsets in the output amplifier.

Offset-Error

Offset error is a measure of the difference between V_{OUT} (actual) and V_{OUT} (ideal) expressed in mV in the linear region of the transfer function. Offset error is measured when Code 32 is loaded into the DAC register.

Gain Error

Gain Error is specified in the linear region of the output range between $V_{out} = 10\text{mV}$ and $V_{out} = AV_{dd} - 50\text{mV}$. It is the deviation in slope of the DAC transfer characteristic from ideal and is expressed in % FSR.

DC Crosstalk

This is the DC change in the output level of one DAC at midscale in response to a fullscale code (all 0's to all 1's and vice versa) and output change of all other DACs. It is expressed in LSbs.

DC Output Impedance

This is the effective output source resistance. It is dominated by package lead resistance.

Output Voltage Settling Time

This is the amount of time it takes for the output of a DAC to settle to a specified level for a 1/4 to 3/4 full-scale input change and measured from $\overline{\text{BUSY}}$ rising edge.

Digital-to-Analog Glitch Energy

This is the amount of energy injected into the analog output at the major code transition. It is specified as the area of the glitch in nV-s. It is measured by toggling the DAC register data between 7FFHex and 800Hex.

DAC-to-DAC Crosstalk

DAC-to-DAC crosstalk is defined as the glitch impulse that appears at the output of one DAC output due to both the digital change and subsequent analog O/P change at another DAC. The victim channel is loaded with mid-scale and DAC-to-DAC crosstalk is specified in nV-s.

Digital Crosstalk

The glitch impulse transferred to the output of one converter due to a change in the DAC register code of another converter is defined as the digital crosstalk and is specified in nV-s.

Digital Feedthrough

When the device is not selected, high frequency logic activity on the device's digital inputs can be capacitively coupled both across and through the device to show up as noise on the V_{OUT} pins. It can also be coupled along the supply and ground lines. This noise is digital feedthrough.

Output Noise Spectral Density

This is a measure of internally generated random noise. Random noise is characterized as a spectral density (voltage per root Hertz). It is measured by loading all DACs to midscale and measuring noise at the output. It is measured in $\text{nV}/(\text{Hz})^{1/2}$ in a 1 Hz bandwidth at 10KHz.

FUNCTIONAL DESCRIPTION

DAC Architecture — General

The AD5381 is a complete single supply, 40-channel, voltage output DAC offering 12-bit resolution, available in a 100 lead LQFP package and features both a parallel and serial interfaces. This family includes an internal 1.25/2.5V, 10ppm/°C reference that can be used to drive the buffered reference inputs, alternatively an external reference can be used to drive these inputs. Reference selection is via a bit in the control register. All channels have an on-chip output amplifier with rail-to-rail output capable of driving a 5kΩ ohm in parallel with a 200pf load.

The architecture of a single DAC channel consists of a 12-bit resistor-string DAC followed by an output buffer amplifier operating at a gain of two. This resistor-string architecture guarantees DAC monotonicity. The 12-bit binary digital code loaded to the DAC register determines at what node on the string the voltage is tapped off before being fed to the output amplifier. Each channel on these devices contains independent offset and gain control registers allowing the user to digitally trim offset and gain. The inclusion of these registers allows the user the ability

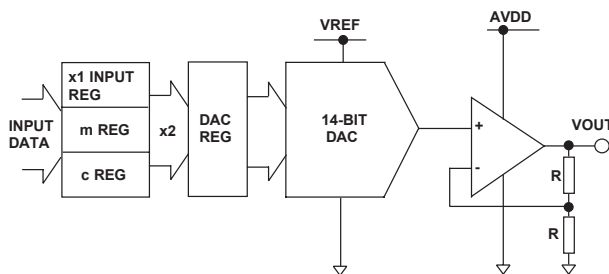


Figure 7. Single Channel Architecture

to calibrate out errors in the complete signal chain including the DAC using the internal M and C registers which hold the correction factors. All channels are double buffered allowing synchronous updating of all channels using the \overline{LDAC} pin. Figure 7 shows a block diagram of a single channel on the AD5381.

The digital input transfer function for each DAC can be represented as:

$$x2 = [(m + 1) / 2^n \times x1] + (c \cdot 2^{n-1})$$

$x2$ is the Dataword loaded to the resistor string DAC

$x1$ is the 12-bit Dataword written to the DAC input register.

m is the 12-bit Gain Coefficient (default is all FFE Hex on the AD5381). The LSB of the 12 bit gain coefficient must always be zero.

n =DAC resolution ($n=12$ for AD5381)

c is the 12-bit Offset Coefficient (default is 800Hex on the AD5381)

The complete transfer function for these devices can be represented as:

$$VOUT = 2 \times V_{REF} \times x2 / 2^n$$

$x2$ is the Dataword loaded to the resistor string DAC
 V_{REF} is the reference voltage applied to the DAC, 2.5V for specified performance.

Data Decoding

The AD5381 contains a 12-bit data bus, DB11-DB0. Depending on the value of REG1 and REG0 outlined in Table 1, this data is loaded into the addressed DAC input register(s), Offset (c) register(s), or Gain (m) register(s). The format data, Offset (c) and gain (m) register contents are outlined in tables II to IV.

Table I. Register Selection

REG1	REG0	Register Selected
1	1	Input Data Register (x1)
1	0	Offset Register (c)
0	1	Gain Register (m)
0	0	Special Function Registers (SFRs)

Table II. DAC Data format (REG1 = 1, REG0 = 1)

DB11 to DB0	DAC Output
1111 1111 1111	$2 V_{REF} \times (4095/4096)V$
1111 1111 1110	$2 V_{REF} \times (4094/4096)V$
1000 0000 0001	$2 V_{REF} \times (2049/4096)V$
1000 0000 0000	$2 V_{REF} \times (2048/4096)V$
0111 1111 1111	$2 V_{REF} \times (2047/4096)V$
0000 0000 0001	$2 V_{REF} \times (1/4096)V$
0000 0000 0000	0V

Table III. Offset Data format (REG1 = 1, REG0 = 0)

DB11 to DB0	Offset
1111 1111 1111	+2047 LSB
1111 1111 1110	+2046 LSB
1000 0000 0001	+1 LSB
1000 0000 0000	+0 LSB
0111 1111 1111	-1 LSB
0000 0000 0001	-2047 LSB
0000 0000 0000	-2048 LSB

Table IV. Gain Data format (REG1 = 0, REG0 = 1)

DB11 to DB0	Gain Factor
1111 1111 1110	1
1011 1111 1110	0.75
0111 1111 1110	0.5
0011 1111 1110	0.25
0000 0000 0000	0

AD5381

AD5381 On-chip Special Function Registers (SFR)

The AD5381 contains a number of special function registers (SFRs) as outlined in table VIII. SFRs are addressed with REG1=REG0= 0 and are decoded using the Address bits A5 to A0.

Table VIII. SFR Register Functions (REG1 =0, REG0 = 0)

R/ \overline{W}	A5	A4	A3	A2	A1	A0	Function
X	0	0	0	0	0	0	NOP (No Operation)
0	0	0	0	0	0	1	Write CLR Code
0	0	0	0	0	1	0	Soft CLR
0	0	0	1	0	0	0	Soft Power Down
0	0	0	1	0	0	1	Soft Power Up
0	0	0	1	1	0	0	Control Register Write
1	0	0	1	1	0	0	Control Register Read
0	0	0	1	0	1	0	Monitor Channel
0	0	0	1	1	1	1	Soft Reset

SFR Commands**NOP** (no operation)

REG1=REG0=0, A5-A0=000000

Performs no operation but is useful in readback mode to clock out data on Dout for diagnostic purposes.

Write CLR Code

REG1=REG0=0, A5-A0=000001

DB11-DB0= Contain the CLR data.

Bringing the $\overline{\text{CLR}}$ line low or exercising the soft clear function will load the contents of the DAC registers with the data contained in the user configurable CLR register and sets VOUT0-VOUT39 accordingly. This can be very useful not only for setting up a specific output voltage in a clear condition but can also be used for calibration purposes where the user can load fullscale or zeroscale to the the clear code register and then issue a hardware or software clear to load this code to all DAC removing the need for individual writes to all DACs. Default on power up is all zeroes.

Soft CLR

REG1=REG0=0, A5-A0=000010

DB11-DB0= Dont Care.

Executing this instruction performs the CLR which is functionally the same as that provided by the external CLR pin. The DAC outputs are loaded with the data in the CLR code register. The time taken to fully execute the SOFT CLR is 80*400ns and is indicated by the $\overline{\text{BUSY}}$ low time.

Soft Power Down

REG1=REG0=0, A5-A0=001000

DB11-DB0= Dont Care.

Executing this instruction performs a global power-down feature that puts all channels into a low power mode reducing both analog and digital power consumption to 5uA. In power down mode the output amplifier can be configured as a high impedance output or provide a 100k load to ground. The contents of all internal registers are retained in power-down mode. Cannot write to any register while in power down.

Soft Power up

REG1=REG0=0, A5-A0=001001

DB11-DB0= Dont Care.

This instruction is used to power up the output amplifiers and internal reference. The time to exit power down is XXus. The hardware power down and software function are internally combined in a digital OR function.

AD5381 Control Register Contents

MSB										LSB
CR11	CR10	CR9	CR8	CR7	CR6	CR5	CR4	CR3	CR1	CR0

Table IX AD5381 Control Register Contents

CR11: Power Down Status. This bit is used to configure the output amplifier state in power down.

CR11=1 amplifier output is high impedance (default on power up).

CR11=0 amplifier output is 100k to ground.

CR10: REF Select. This bit selects the operating internal reference for the AD5381. CR10 is programmed as follows:

CR10=1: Internal reference is 2.5V (default on power-up). Recommended reference for 5V operation.

CR10=0: Internal reference is 1.25V. Recommended reference for 3V operation.

CR9: Current Boost Control. This bit is used to boost the current in the output amplifier thereby altering its settling time. This bit is configured as follows:

CR9=1: Boost mode on. This maximizes the bias current in the output amplifier giving the fastest settling time (2 μ s typ) but increasing the power dissipation.

CR9=0: Boost mode off (default on power up). This reduces the bias current in the output amplifier and reduces the overall power consumption but increases the settling time to 6 μ s typ.

CR8: Internal/External Reference. This bit determines if the DAC uses its internal reference or an externally applied reference.

CR8=1: Internal Reference enabled. 1.25V with 3V supplies and 2.5V with 5V supplies.

CR8=0: External Reference selected (default on power up)

CR7: Voltage Output Monitor Enable

CR7=1: Monitor Enabled. This enables the channel monitor function. Following a write to the monitor channel in the SFR register the selected channel output is routed to the MON_OUT pin. VOUT 39 operates as the MON-OUT pin on the 40-channel device.

CR7=0: Monitor Disabled (default on power-up). When monitor is disabled the MON_OUT pin is tristated on the 32-channel devices and VOUT 39 assumes its normal DAC output function on the 40-channel device.

CR6: Thermal Monitor Function. This function is used to monitor the internal die temperature of the AD5381 devices when enabled. The thermal monitor puts the device into soft power down when the temperature exceeds 130 degree C. This function can be used to protect the device in cases where the power dissipation of the device may be exceeded if a number of output channels are simultaneously short circuited.

CR6=1: Monitor enabled

CR6=0 Monitor disabled (default on power-up).

CR5-CR0: These are don't care conditions.

Soft RESET

REG1=REG0=0, A5-A0=001111

DB11-DB0= Don't Care.

This instruction is used to implement a software reset. All internal registers are reset to their default values which corresponds to m at fullscale and c at zero. The contents of the DAC registers are cleared setting all analog outputs to zero volts. The soft reset activation time is 150 μ s (typ).

Monitor Channel

REG1=REG0=0, A5-A0=001010

DB11-DB6= Contain data to address the channel to be monitored.

A monitor function is provided on all devices. This feature consisting of a multiplexer addressed via the interface allows any channel output to be routed to this pin for monitoring using an external ADC. In channel monitor mode Vout 39 becomes the MON_OUT pin, the pin to which all monitored pins are routed. The channel monitor function must be enabled in the control register before any channels are routed to the MON_OUT pin. On the AD5381, DB11 to DB6 contain the channel address for the monitored channel. Selecting channel 63 tristates the MON_OUT pin.

The Channel Address decoding for the AD5381:

AD5381

REG1	REG0	A5	A4	A3	A2	A1	A0	DB11	DB10	DB9	DB8	DB7	DB6	DB5 ->DB0	AD5381	MON_OUT
0	0	0	0	1	0	1	0	0	0	0	0	0	0	X	Vout 0	
0	0	0	0	1	0	1	0	0	0	0	0	0	1	X	Vout 1	
0	0	0	0	1	0	1	0	0	0	0	0	1	0	X	Vout 2	
0	0	0	0	1	0	1	0	0	0	0	0	1	1	X	Vout 3	
0	0	0	0	1	0	1	0	0	0	0	1	0	0	X	Vout 4	
0	0	0	0	1	0	1	0	0	0	0	1	0	1	X	Vout 5	
0	0	0	0	1	0	1	0	0	0	0	1	1	0	X	Vout 6	
0	0	0	0	1	0	1	0	0	0	0	1	1	1	X	Vout 7	
0	0	0	0	1	0	1	0	0	0	1	0	0	0	X	Vout 8	
0	0	0	0	1	0	1	0	0	0	1	0	0	1	X	Vout 9	
0	0	0	0	1	0	1	0	0	0	1	0	1	0	X	Vout 10	
0	0	0	0	1	0	1	0	0	0	1	0	1	1	X	Vout 11	
0	0	0	0	1	0	1	0	0	0	1	1	0	0	X	Vout 12	
0	0	0	0	1	0	1	0	0	0	1	1	0	1	X	Vout 13	
0	0	0	0	1	0	1	0	0	0	1	1	1	0	X	Vout 14	
0	0	0	0	1	0	1	0	0	0	1	1	1	1	X	Vout 15	
0	0	0	0	1	0	1	0	0	1	0	0	0	0	X	Vout 16	
0	0	0	0	1	0	1	0	0	1	0	0	0	1	X	Vout 17	
0	0	0	0	1	0	1	0	0	1	0	0	1	0	X	Vout 18	
0	0	0	0	1	0	1	0	0	1	0	0	1	1	X	Vout 19	
0	0	0	0	1	0	1	0	0	1	0	1	0	0	X	Vout 20	
0	0	0	0	1	0	1	0	0	1	0	1	0	1	X	Vout 21	
0	0	0	0	1	0	1	0	0	1	0	1	1	0	X	Vout 22	
0	0	0	0	1	0	1	0	0	1	1	0	1	1	X	Vout 23	
0	0	0	0	1	0	1	0	0	1	1	0	0	0	X	Vout 24	
0	0	0	0	1	0	1	0	0	1	1	0	0	1	X	Vout 25	
0	0	0	0	1	0	1	0	0	1	1	0	1	0	X	Vout 26	
0	0	0	0	1	0	1	0	0	1	1	0	1	1	X	Vout 27	
0	0	0	0	1	0	1	0	0	1	1	1	0	0	X	Vout 28	
0	0	0	0	1	0	1	0	0	1	1	1	0	1	X	Vout 29	
0	0	0	0	1	0	1	0	0	1	1	1	1	0	X	Vout 30	
0	0	0	0	1	0	1	0	0	1	1	1	1	1	X	Vout 31	
0	0	0	0	1	0	1	0	1	0	0	0	0	0	X	Vout 32	
0	0	0	0	1	0	1	0	1	1	0	0	0	1	X	Vout 33	
0	0	0	0	1	0	1	0	1	1	0	0	1	0	X	Vout 34	
0	0	0	0	1	0	1	0	1	1	0	0	1	1	X	Vout 35	
0	0	0	0	1	0	1	0	1	1	0	1	0	0	X	Vout 36	
0	0	0	0	1	0	1	0	1	1	0	1	0	1	X	Vout 37	
0	0	0	0	1	0	1	0	1	1	0	1	1	0	X	Vout 38	
0	0	0	0	1	0	1	0	1	1	1	X	X	X	X	Undefined	
0	0	0	0	1	0	1	0	1	1	1	1	1	1	X	Tristate	

Table X. AD5381 Channel Monitor Decoding

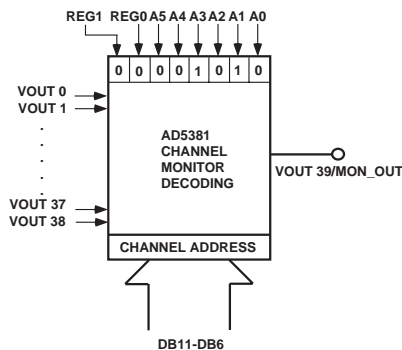


Figure 8. AD5381 Channel Monitor Decoding

Hardware Functions

Reset Function

Bringing the $\overline{\text{RESET}}$ line low resets the contents of all internal registers to their power-on-reset state. Reset is a negative edge sensitive input. The default corresponds to m at fullscale and c at zero. The contents of the DAC registers are cleared setting VOUT0-VOUT39 to zero volts. This sequence takes 300us (typ). The falling edge of $\overline{\text{RESET}}$ initiates the reset process and $\overline{\text{BUSY}}$ goes low for the duration returning high when $\overline{\text{RESET}}$ is complete. While $\overline{\text{BUSY}}$ is low all interfaces are disabled and all $\overline{\text{LDAC}}$ pulses are ignored. When $\overline{\text{BUSY}}$ returns high the part resumes normal operation and the status of the $\overline{\text{RESET}}$ pin is ignored till the next falling edge is detected.

Asynchronous Clear Function

Bringing the $\overline{\text{CLR}}$ line low clears the contents of the DAC registers to the data contained in the user configurable CLR register and sets VOUT0-VOUT39 accordingly. This function can be used in system calibration to load zeroscale and fullscale to all channels together. The execution time for a CLR is 32us.

$\overline{\text{BUSY}}$ and $\overline{\text{LDAC}}$ Functions

$\overline{\text{BUSY}}$ is a digital cmos output indicating the status of the AD538X devices. $\overline{\text{BUSY}}$ goes low during internal calculations of x2 data. During this time the user can continue writing new data to further x1, c and m registers in parallel interface mode and these are stored in a FIFO but no updates to the DAC registers and DAC outputs will take place. If $\overline{\text{LDAC}}$ is taken low while $\overline{\text{BUSY}}$ is low this event is stored.

$\overline{\text{BUSY}}$ also goes low during power-on-reset and on a falling edge is detected on the $\overline{\text{RESET}}$ pin. During this time all interfaces are disabled and any events on $\overline{\text{LDAC}}$ are ignored.

The AD5381 contain an extra feature whereby a DAC register is not updated unless it's x2 register has been written to since the last time $\overline{\text{LDAC}}$ was brought low. Normally, when $\overline{\text{LDAC}}$ is brought low, the DAC registers are filled with the contents of the x2 registers. However these devices will only update the DAC register if the x2 data has changed, thereby removing unnecessary digital crosstalk.

Power-On-Reset

The AD5381 contains a power-on-reset generator and state-machine. The power-on-reset resets all registers to a predefined state and the analog outputs are configured with a 100k impedance to ground. The $\overline{\text{BUSY}}$ pin goes low during the power-on-reset sequencing preventing data writes to the device.

Power-Down

The AD5381 contains a global power-down feature that puts all channels into a low power mode reducing both analog and digital power consumption to 5uA. In power down mode the output amplifier can be configured as a high impedance output or provide a 100k load to ground. The contents of all internal registers are retained in power-down mode. When exiting power down the settling time of the amplifier will elapse before the outputs settle to their correct value.

INTERFACES

The AD5381 contains both a parallel and serial interfaces. Furthermore, the serial interface can be programmed to be either DSP, SPI, MICROWIRE or I2C compatible. The SER/PAR pin selects parallel and serial interface modes. In serial mode SPI/I2C pin is used to select DSP, SPI, MICROWIRE or I2C interface mode.

The devices use an internal FIFO memory to allow high speed successive writes in parallel interface mode. The user can continue writing new data to the device while write instructions are being executed. The $\overline{\text{BUSY}}$ signal indicates the current status of the device, going low while instructions in the FIFO are being executed. Up to 128 successive instructions can be written to the FIFO at maximum speed in parallel mode. When the FIFO is full any further writes to the device are ignored.

To minimize both the power consumption of the device and on-chip digital noise, the active interface only powers up fully when the device is being written to, i.e. on the falling edge of $\overline{\text{WR}}$ or on the falling edge of $\overline{\text{SYNC}}$.

DSP, SPI, MICROWIRE Compatible Serial Interface

The serial interface can be operated with a minimum of 3-wires in stand alone mode or 5-wires in daisy chain mode. Daisy chaining allows many devices to be cascaded together to increase system channel count. The SER/PAR pin must be tied high and the $\overline{\text{SPI/I2C}}$ (pin 97) should be tied low to enable the DSP, SPI, MICROWIRE compatible serial interface. In serial interface mode the user does not need to drive the parallel input data pins. The serial interface is control pins are as follows:

$\overline{\text{SYNC}}$, DIN, SCLK - Standard 3-wire interface pins.

DCEN - Selects Stand-Alone Mode or Daisy-Chain Mode.

SDO - Data Out pin for Daisy-Chain Mode.

Figures 3 and 4 show the timing diagram for a serial write to the AD5381 in both Stand-Alone and Daisy-Chain Mode.

The 24-bit data word format for the serial interface is shown in Figure 9 below.

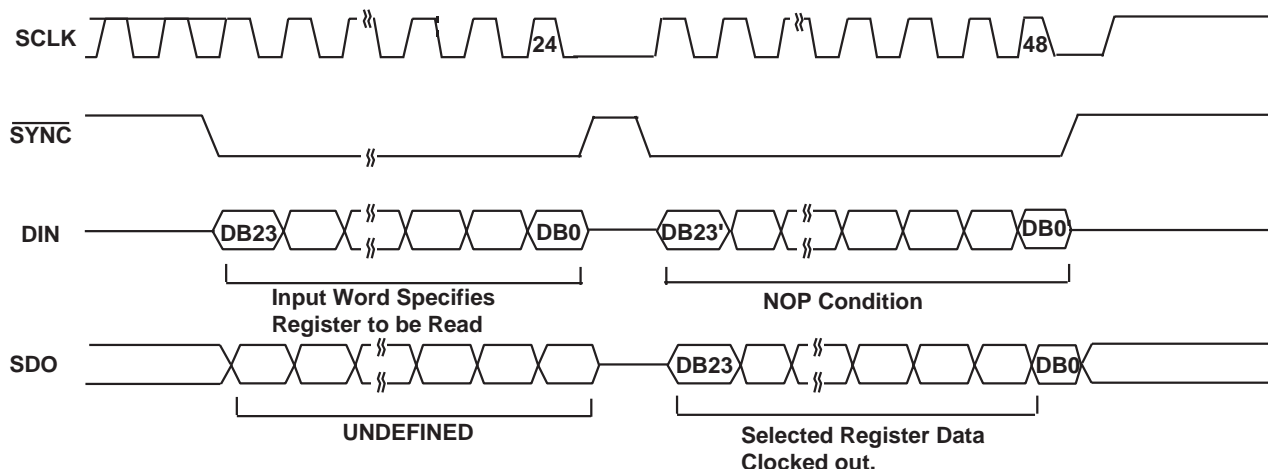


Figure 10. AD5381, SPI Readback Operation

I2C Serial Interface

The AD5381 feature an I2C compatible 2-wire interface consisting of a serial data line (SDA) and a serial clock line (SCL). SDA and SCL facilitate communication between the AD5381 and the master at rates up to 400kHz. Figure 5 shows the I2C interface timing while figures 11,12 and 13 show the 2-wire interface incorporating three different modes of operation.

In selecting the I2C operating mode firstly configure serial operating mode ($SER/\overline{PAR}=1$) and then select I2C mode by configuring the $\overline{SPI/I2C}$ pin to a logic 1. The device is connected to this bus as slave devices (i.e., no clock is generated by the AD5381). The AD5381 has a 7-bit slave address 1010 1AD1AD0. The 5 MSBs are hard coded and the two LSBs are determined by the state of the AD1 AD0 pins. The facility to hardware configure AD1 and AD0 allows four of these devices to be configured on the bus.

I2C Data Transfer

One data bit is transferred during each SCL clock cycle. The data on SDA must remain stable during the high period of the SCL clock pulse. Changes in SDA while SCL is high are control signals that configure START and STOP Conditions. Both SDA and SCL are pulled high by the external pull-up resistors when the I2C bus is not busy.

START and STOP Conditions

A master device initiates communication by issuing a START condition. A START condition is a high-to-low transition on SDA with SCL high. A STOP condition is a low-to-high transition on SDA, while SCL is high.

A START condition from the master signals the beginning of a transmission to the AD538X. The STOP condition frees the bus. If a repeated START condition (S_r) is generated instead of a STOP condition, the bus remains active.

Repeated START Conditions

A repeated START (S_r) condition may indicate a change of data direction on the bus. S_r may be used when the bus master is writing to several I2C devices and does not want to relinquish control of the bus.

Acknowledge Bit (ACK)

The acknowledge bit (ACK) is the ninth bit attached to any 8-bit data word. ACK is always generated by the receiving device. The AD5381 devices generate an ACK when receiving an address or data by pulling SDA low during the ninth clock period. Monitoring ACK allows for detection of unsuccessful data transfers. An unsuccessful data transfer occurs if a receiving device is busy or if a system fault has occurred. In the event of an unsuccessful data transfer, the bus master should reattempt communication.

AD5381 Slave Addresses

A bus master initiates communication with a slave device by issuing a START condition followed by the 7-

bit slave address. When idle, the AD5381 waits for a START condition followed by its slave address. The LSB of the address word is the Read/Write (R/\overline{W}) bit. The AD5381 device is a receive only device when communicating with this $R/\overline{W} = 0$. After receiving the proper address 1010 1AD1AD0, the AD5381 issues an ACK by pulling SDA low for one clock cycle. The AD5381 has four different user programmable addresses determined by the AD1 and AD0 bits.

3-Byte Mode

Three byte mode allows the user update more than one channel in a write sequence without having to write the device address byte each time. The device address byte is only required once and subsequent channel updates require the pointer byte and the data bytes. In three byte mode the user begins with an address byte ($R/\overline{W} = 0$) after which the DAC will acknowledge that it is prepared to receive data by pulling SDA low. The address byte is followed by the pointer byte, this addresses the specific channel in the DAC to be addressed and is also acknowledged by the DAC. This is then followed by the two data bytes. REG1 and REG0 determine the register to be updated.

If a STOP condition is not sent following the data bytes another channel can be updated by sending a new pointer byte followed by the data bytes. This mode only requires 3-bytes to be sent to update any channel once the device has been initially addressed and reduces the software overhead in updating the AD5381 channels. A STOP condition at any time exits this mode. Figure 12 shows a typical configuration.

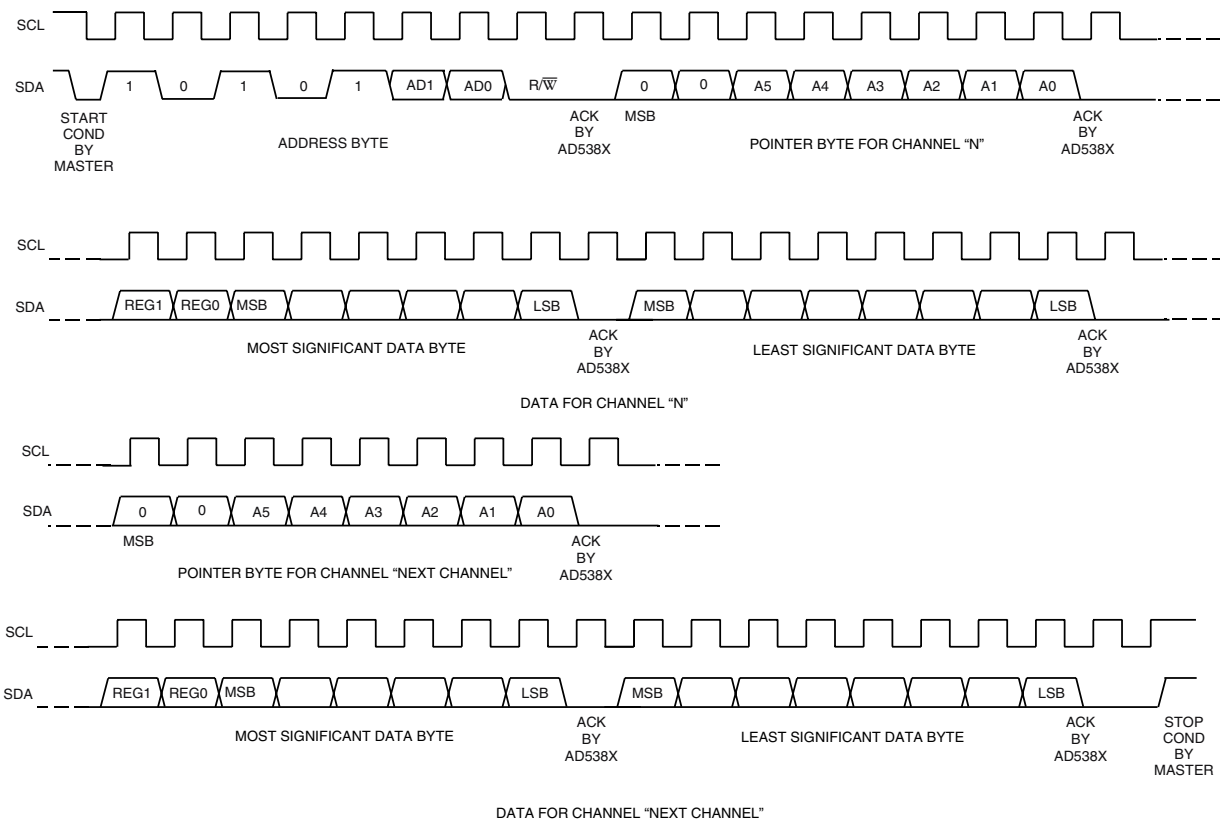


Figure 12 . 3-Byte AD5381, I2C Write Operation

AD5381

2-Byte Mode

Two byte mode allows the user update channels sequentially following initialization of this mode. The device address byte is only required once and the pointer address pointer is configured for auto increment or burst mode. The user must begin with an address byte ($R/\overline{W} = 0$) after which the DAC will acknowledge that it is prepared to receive data by pulling SDA low. The address byte is followed by a specific pointer byte (3F Hex) which initiates the burst mode of operation. In this mode the address pointer initializes to channel zero and automatically increments to the next address on receiving the two data bytes for the present address. The REG0 and REG 1 bits in the data byte determine the register to be updated. In this mode, following the initialization only the 2-data bytes are required to update a channel, the channel address automatically increments from address 0. This allows transmission of data to all channels in one block and reduces the software overhead in configuring all channels. A STOP condition at any time exits this mode. Figure 13 shows a typical configuration.

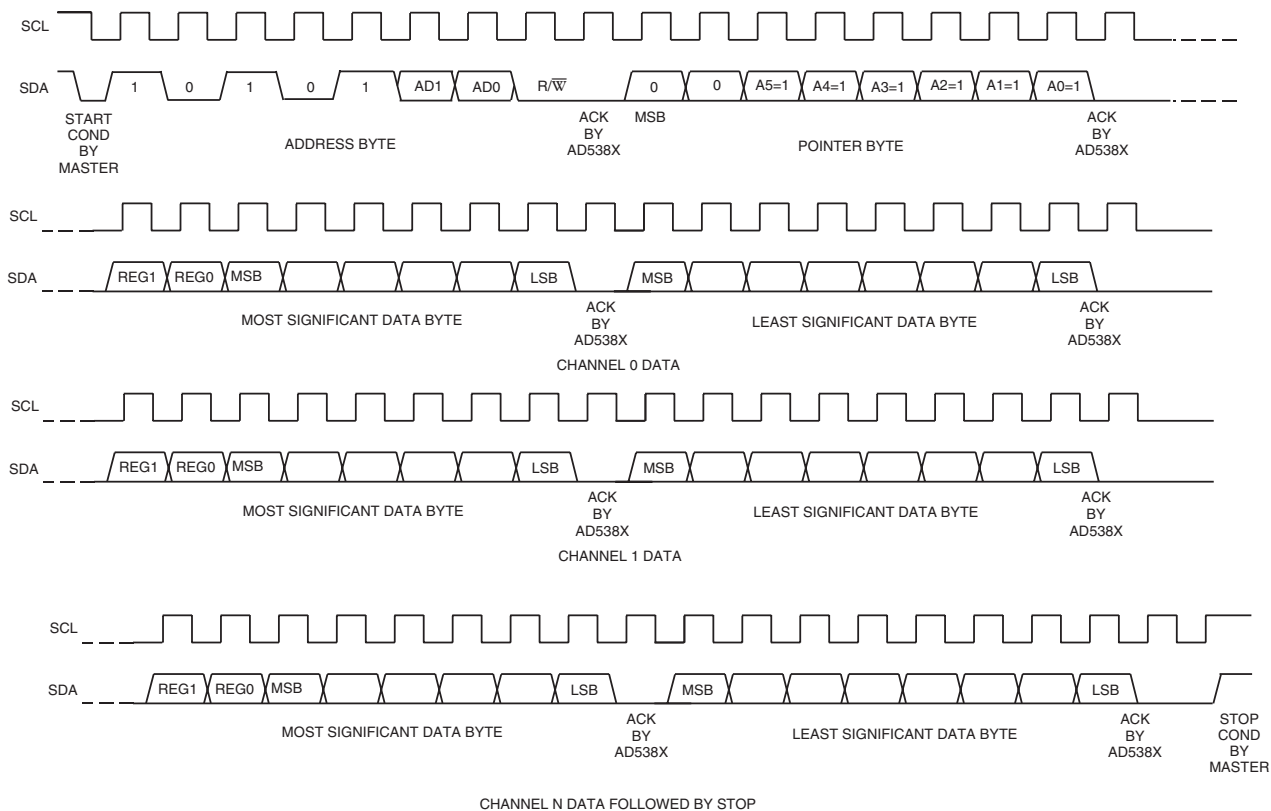


Figure 13 . 2-Byte AD5381, I2C Write Operation

Parallel Interface

The SER/ \overline{PAR} pin must be tied low to enable the parallel interface and disable the serial interfaces. Figure 5 shows the timing diagram for a parallel write. The parallel interface is controlled by the following pins:

\overline{CS} Pin

Active low device select pin.

\overline{WR} Pin

On the rising edge of \overline{WR} , with \overline{CS} low, the address on pins A5-A0 are latched and data present on the data bus is loaded into the selected input registers.

REG0, REG1 Pins

The REG0 and REG1 pins determine the destination register of the data being written to the AD5380/82. See Table I.

A5-A0 Pins

Each of the 40 DAC channels can be addressed individually.

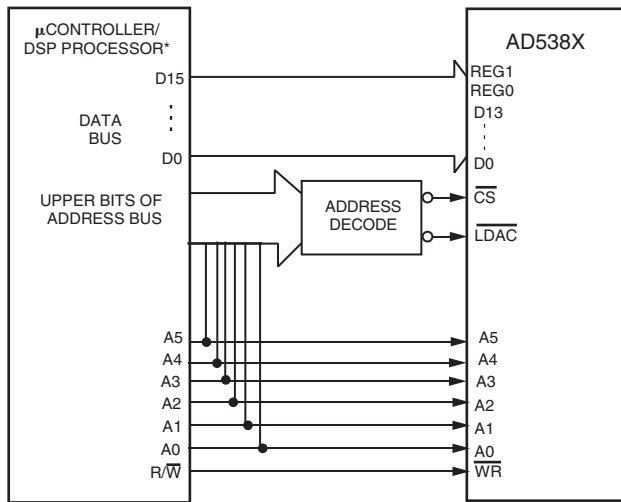
DB11-DB0 Pins

The AD5381 accepts a straight 12-bit parallel word on DB11-DB0 where DB11 is the MSB and DB0 is the LSB.

Microprocessor Interfacing

Parallel Interface

The AD5381 can be interfaced to a variety of 16-bit microcontrollers or DSP processors. Figure X shows the AD5381 family interfaced to a generic 16-bit microcontroller/DSP processor. The lower address lines from the processor are connected to A0 to A5 on the AD5381 as shown. The upper address lines are decoded to provide a CS, LDAC signals for the AD5381. The fast interface timing of the AD5381 allows direct interface to a wide variety of microcontrollers and DSPs as shown in Figure 14.



*ADDITIONAL PINS OMITTED FOR CLARITY

Figure 14 . AD5381 Parallel Interface

AD5381 to MC68HC11

The Serial Peripheral Interface (SPI) on the MC68HC11 is configured for Master Mode (MSTR = 1), Clock Polarity Bit (CPOL) = 0 and the Clock Phase Bit (CPHA) = 1. The SPI is configured by writing to the SPI Control Register (SPCR)—see 68HC11 User Manual. SCK of the 68HC11 drives the SCLK of the AD5381, the MOSI output drives the serial data line (D_{IN}) of the AD5381 and the MISO input is driven from D_{OUT}. The SYNC signal is derived from a port line (PC7). When data is being transmitted to the AD5381, the SYNC line is taken low (PC7). Data appearing on the MOSI output is valid on the falling edge of SCK. Serial data from the 68HC11 is transmitted in 8-bit bytes with only eight falling clock edges occurring in the transmit cycle.

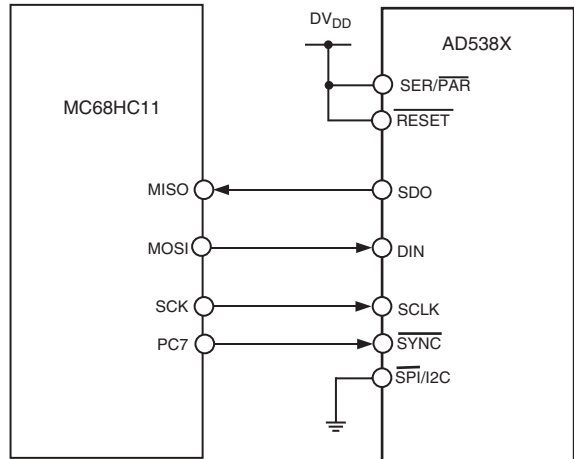


Figure 15 . AD5381 -MC68HC11 Interface

AD5381 to PIC16C6x/7x

The PIC16C6x/7x Synchronous Serial Port (SSP) is configured as an SPI Master with the Clock Polarity bit = 0. This is done by writing to the Synchronous Serial Port Control Register(SSPCON). See user PIC16/17 Microcontroller User Manual. In this example I/O port RA1 is being used to pulse SYNC and enable the serial port of the AD5381. This microcontroller transfers only eight bits of data during each serial transfer operation; therefore, three consecutive read/write operations are needed depending on the mode. Figure 16 shows the connection diagram.

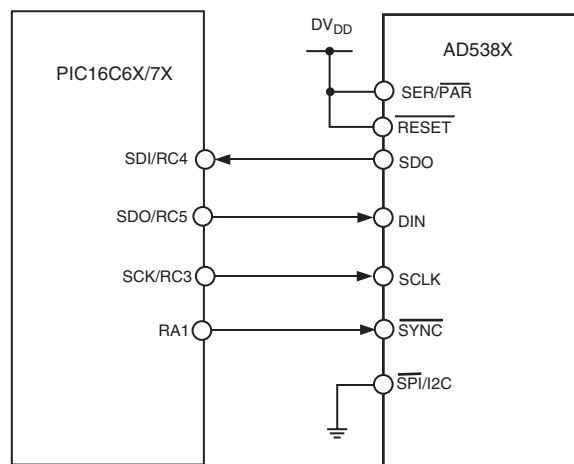


Figure 16 . AD5381 -PIC16C6X/7X Interface

AD5381

AD5381 to 8051

The AD5381 requires a clock synchronized to the serial data. The 8051 serial interface must therefore be operated in Mode 0. In this mode serial data enters and exits through RxD and a shift clock is output on TxD. Figure 23 shows how the 8051 is connected to the AD5381. Because the AD5381 shifts data out on the rising edge of the shift clock and latches data in on the falling edge, the shift clock must be inverted. The AD5381 requires its data with the MSB first. Since the 8051 outputs the LSB first, the transmit routine must take this into account.

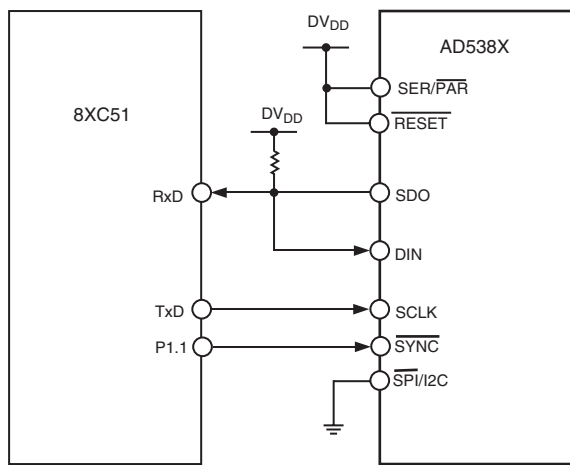


Figure 17. AD5381 - 8051 Interface

AD5381 to ADSP2101/2103

Figure 18 shows a serial interface between the AD5381 and the ADSP-2101/ADSP-2103. The ADSP-2101/ADSP-2103 should be set up to operate in the SPORT Transmit Alternate Framing Mode. The ADSP-2101/ADSP-2103 SPORT is programmed through the SPORT control register and should be configured as follows: Internal Clock Operation, Active Low Framing, 16-Bit Word Length. Transmission is initiated by writing a word to the Tx register after the SPORT has been enabled.

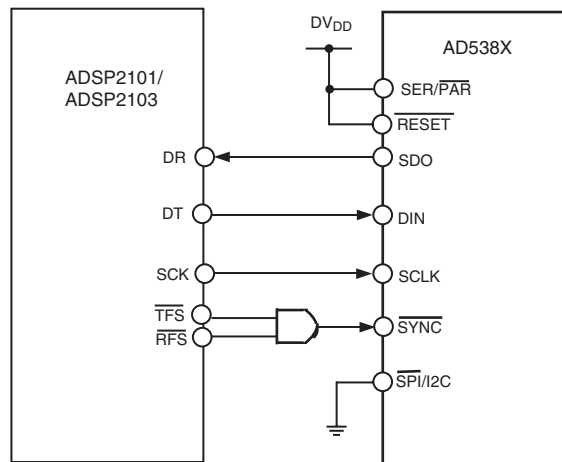


Figure 18. AD5381 -ADSP2101/ADSP3103 Interface

POWER SUPPLY DECOUPLING

In any circuit where accuracy is important, careful consideration of the power supply and ground return layout helps to ensure the rated performance. The printed circuit board on which the AD5381 is mounted should be designed so that the analog and digital sections are separated, and confined to certain areas of the board. If the AD5381 is in a system where multiple devices require an AGND-to-DGND connection, the connection should be made at one point only. The star ground point should be established as close as possible to the device. For supplies with multiple pins (AV_{DD} , AV_{CC}) it is recommended to tie those pins together. The AD5381 should have ample supply bypassing of 10 μF in parallel with 0.1 μF on each supply located as close to the package as possible, ideally right up against the device. The 10 μF capacitors are the tantalum bead type. The 0.1 μF capacitor should have low Effective Series Resistance (ESR) and Effective Series Inductance (ESI), like the common ceramic types that provide a low impedance path to ground at high frequencies, to handle transient currents due to internal logic switching.

The power supply lines of the AD5381 should use as large a trace as possible to provide low impedance paths and reduce the effects of glitches on the power supply line. Fast switching signals such as clocks should be shielded with digital ground to avoid radiating noise to other parts of the board, and should never be run near the reference inputs. A ground line routed between the D_{IN} and SCLK lines will help reduce crosstalk between them (not required on a multilayer board as there will be a separate ground plane, but separating the lines will help). It is essential to minimize noise on V_{IN} and REFIN lines.

Avoid crossover of digital and analog signals. Traces on opposite sides of the board should run at right angles to each other. This reduces the effects of feedthrough through the board. A microstrip technique is by far the best, but not always possible with a double-sided board. In this technique, the component side of the board is dedicated to ground plane while signal traces are placed on the solder side.

OUTLINE DIMENSIONS

ST100 (100 Lead LQFP) Package Dimensions

