ANALOG DEVICES

Differential Input, 555kSPS, 12-Bit ADC in an 8-lead SOT-23

Preliminary Technical Data AD7452

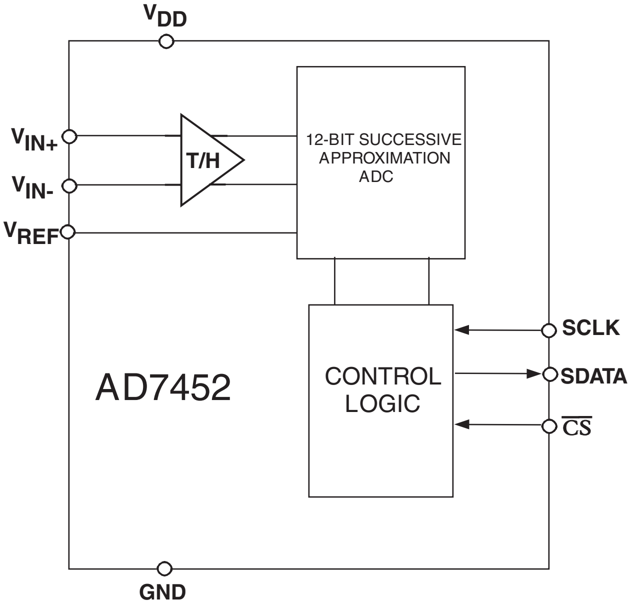
FEATURES

Specified for V_{DD} of 3 V and 5 V
Low Power at max Throughput Rate:
  7.25 mW max at 555kSPS with 3 V Supplies
  3.3 mW max at 555kSPS with 5 V Supplies
Fully Differential Analog Input
Wide Input Bandwidth:
  70dB SINAD at 100kHz Input Frequency
Flexible Power/Serial Clock Speed Management
No Pipeline Delays
High Speed Serial Interface - SPI™/QSPI™/ MICROWIRE™/ DSP Compatible
Power-Down Mode: 1μA max
8 Lead SOT-23 and MSOP Packages

APPLICATIONS

Transducer Interface
Battery Powered Systems
Data Acquisition Systems
Portable Instrumentation
Motor Control
Communications

FUNCTIONAL BLOCK DIAGRAM



GENERAL DESCRIPTION

The AD7452 is a 12-bit, low power, successive-approximation (SAR) analog-to-digital converter that features a fully differential analog input. This part operates from a single 3 V or 5 V power supply and features throughput rates up to 555kSPS.

The part contains a low-noise, wide bandwidth, differential track and hold amplifier (T/H) which can handle input frequencies in excess of 1MHz. The reference voltage is applied externally to the V_{REF} pin and can be varied from 100 mV to 3.5 V depending on the power supply and what suits the application. The value of the reference voltage determines the common mode voltage range of the part. With this truly differential input structure and variable reference input, the user can select a variety of input ranges and bias points.

The conversion process and data acquisition are controlled using $\overline{CS}$ and the serial clock allowing the device to interface with Microprocessors or DSPs. The input signals are sampled on the falling edge of $\overline{CS}$ and the conversion is also initiated at this point.

The SAR architecture of these parts ensures that there are no pipeline delays.

The AD7452 uses advanced design techniques to achieve very low power dissipation.

PRODUCT HIGHLIGHTS

1. Operation with either 3 V or 5 V power supplies.
2. Low Power Consumption.
   With a 3V supply, the AD7452 offers 3.3 mW max power consumption for 555kSPS throughput.
3. Fully Differential Analog Input.
4. Flexible Power/Serial Clock Speed Management.
   The conversion rate is determined by the serial clock, allowing the power to be reduced as the conversion time is reduced through the serial clock speed increase. These parts also feature a shutdown mode to maximize power efficiency at lower throughput rates.
5. Variable Voltage Reference Input.
6. No Pipeline Delay.
7. Accurate control of the sampling instant via a $\overline{CS}$ input and once off conversion control.
8. ENOB > 8 Bits typically for a 100mV reference.

MICROWIRE is a trademark of National Semiconductor Corporation.
SPI and QSPI are trademarks of Motorola, Inc.

REV. PrE 26 May 2003

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AD7452 - SPECIFICATIONS[1]

(V_{DD} = 2.7V to 3.6V, f_{SCLK} = 10MHz, f_S = 555kSPS, V_{REF} = 2.0 V;
V_{DD} = 4.75V to 5.25V, f_{SCLK} = 10MHz, f_S = 555kSPS, V_{REF} = 2.5 V;
V_{CM}[2] = V_{REF}; T_A = T_{MIN} to T_{MAX}, unless otherwise noted.)

Parameter	Test Conditions/Comments	B Version[1]	Unit
DYNAMIC PERFORMANCE	F_{IN} = 100kHz		
Signal to (Noise + Distortion) (SINAD)[3]	V_{DD} = 4.75V to 5.25V	70	dB min
	V_{DD} = 2.7V to 3.6V	68	dB min
Total Harmonic Distortion (THD)[3]	V_{DD} = 4.75V to 5.25V, -80dB typ	-75	dB max
	V_{DD} = 2.7V to 3.6V, -78dB typ	-73	dB max
Peak Harmonic or Spurious Noise[3]	V_{DD} = 4.75V to 5.25V, -82dB typ	-75	dB max
	V_{DD} = 2.7V to 3.6V, -80dB typ	-73	dB max
Intermodulation Distortion (IMD)[3]	fa = 90kHz, fb = 110kHz		
Second Order Terms		-83	dB typ
Third Order Terms		-83	dB typ
Aperture Delay[3]		5	ns typ
Aperture Jitter[3]		50	ps typ
Full Power Bandwidth[3]	@ -3 dB	20	MHz typ
	@ -0.1 dB	2.5[4]	MHz typ
DC ACCURACY			
Resolution		12	Bits
Integral Nonlinearity (INL)[3]		±1	LSB max
Differential Nonlinearity (DNL)[3]	Guaranteed No Missed Codes to 12 Bits.	±1	LSB max
Zero Code Error[3]	V_{DD} = 4.75V to 5.25V	±3	LSB max
	V_{DD} = 2.7V to 3.6V	±6	LSB max
Positive Gain Error[3]	V_{DD} = 4.75V to 5.25V	±3	LSB max
	V_{DD} = 2.7V to 3.6V	±6	LSB max
Negative Gain Error[3]	V_{DD} = 4.75V to 5.25V	±3	LSB max
	V_{DD} = 2.7V to 3.6V	±6	LSB max
ANALOG INPUT			
Full Scale Input Span	2 x V_{REF}[5]	V_{IN+} - V_{IN-}	V
Absolute Input Voltage			
V_{IN+}	V_{CM}[2] = V_{REF}	V_{CM}[2] ± $V_{REF}/2$	V
V_{IN-}	V_{CM}[2] = V_{REF}	V_{CM}[2] ± $V_{REF}/2$	V
DC Leakage Current		±1	µA max
Input Capacitance	When in Track/Hold	30/10	pF typ
REFERENCE INPUT			
V_{REF} Input Voltage	V_{DD} = 4.75V to 5.25V (±1% tolerance for specified performance)	2.5[6]	V
	V_{DD} = 2.7V to 3.6V (±1% tolerance for specified performance)	2.0[7]	V
DC Leakage Current		±1	µA max
V_{REF} Input Capacitance	When in Track/Hold	10/30	pF typ
LOGIC INPUTS			
Input High Voltage, V_{INH}		2.4	V min
Input Low Voltage, V_{INL}		0.8	V max
Input Current, I_{IN}	Typically 10nA, V_{IN} = 0VorV$_{DD}$	±1	µA max
Input Capacitance, C_{IN}[8]		10	pF max
LOGIC OUTPUTS			
Output High Voltage, V_{OH}	V_{DD} = 4.75V to 5.25V; I_{SOURCE} = 200µA	2.8	V min
	V_{DD} = 2.7V to 3.6V; I_{SOURCE} = 200µA	2.4	V min
Output Low Voltage, V_{OL}	I_{SINK} =200µA	0.4	V max
Floating-State Leakage Current		±1	µA max
Floating-State Output Capacitance[8]		10	pF max
Output Coding		Two's Complement	

AD7452 - SPECIFICATIONS[1]

Parameter	Test Conditions/Comments	B Version[1]	Units
CONVERSION RATE			
Conversion Time	1.6μs with an 10MHz SCLK	16	SCLK cycles
Track/Hold Acquisition Time[3]	Sine Wave Input	200	ns max
	Step Input	290	ns max
Throughput Rate		555	kSPS max
POWER REQUIREMENTS			
V_{DD}	Range: 3 V+20%/-10%;		
	5 V ± 5%	2.7/5.25	Vmin/max
I_{DD}[9, 10]			
Normal Mode(Static)	SCLK On or Off	0.5	mA typ
Normal Mode (Operational)	V_{DD} = 4.75V to 5.25V.	1.5	mA max
	V_{DD} = 2.7V to 3.6V.	1.2	mA max
Full Power-Down Mode	SCLK On or Off	1	μA max
Power Dissipation			
Normal Mode (Operational)	V_{DD} =5 V. 1.55mW typ for 100kSPS	7.25	mW max
	V_{DD} =3 V. 0.64mW typ for 100kSPS	3.3	mW max
Full Power-Down	V_{DD} =5 V. SCLK On or Off	5	μW max
	V_{DD} =3 V. SCLK On or Off	3	μW max

NOTES

[1] Temperature ranges as follows: B Version: –40°C to +85°C.

[2] Common Mode Voltage. The input signal can be centered on any choice of dc Common Mode Voltage as long as this value is in the range specified in Figures 8 and 9.

[3] See 'Terminology' section.

[4] For input frequencies above 2.5MHz, a correct conversio result cannot be guaranteed

[5] Because the input spans of V_{IN+} and V_{IN-} are both V_{REF}, and they are 180° out of phase, the differential voltage is 2 x V_{REF}.

[6] The AD7452 is functional with a reference input from100mV and for V_{DD} = 5V, the reference can range up to 3.5V.

[7] The AD7452 is functional with a reference input from100mV and for V_{DD} = 3V, the reference range up to 2.2V.

[8] Sample tested @ +25°C to ensure compliance.

[9] See Power vs. Throughput Rate section.

[10] Measured with a midscale DC input.

Specifications subject to change without notice.

TIMING SPECIFICATIONS [1,2]

(V_{DD} = 2.7V to 3.6V, f_{SCLK} = 10MHz, f_S = 555kSPS, V_{REF} = 2.0 V;
V_{DD} = 4.75V to 5.25V, f_{SCLK} = 10MHz, f_S = 555kSPS, V_{REF} = 2.5 V;
V_{CM} [3] = V_{REF}; T_A = T_{MIN} to T_{MAX}, unless otherwise noted.)

Parameter	Limit at T_{MIN}, T_{MAX}	Units	Description
f_{SCLK} [4]	10	kHz min	
	10	MHz max	
$t_{CONVERT}$	16 x t_{SCLK}		t_{SCLK} = 1/f_{SCLK}
	1.6	µs max	
t_{QUIET}	60	ns min	Minimum Quiet Time between the End of a Serial Read and the Next Falling Edge of $\overline{CS}$
t_1	10	ns min	Minimum $\overline{CS}$ Pulsewidth
t_2	10	ns min	$\overline{CS}$ falling Edge to SCLK Falling Edge Setup Time
t_3 [5]	20	ns max	Delay from $\overline{CS}$ Falling Edge Until SDATA 3-State Disabled
t_4 [5]	40	ns max	Data Access Time After SCLK Falling Edge
t_5	0.4 t_{SCLK}	ns min	SCLK High Pulse Width
t_6	0.4 t_{SCLK}	ns min	SCLK Low Pulse Width
t_7	10	ns min	SCLK Edge to Data Valid Hold Time
t_8 [6]	10	ns min	SCLK Falling Edge to SDATA 3-State Enabled
	35	ns max	SCLK Falling Edge to SDATA 3-State Enabled
$t_{POWER-UP}$ [7]	1	µs max	Power-Up Time from Full Power-Down

NOTES

[1] Sample tested at +25°C to ensure compliance. All input signals are specified with tr = tf = 5 ns (10% to 90% of V_{DD}) and timed from a voltage level of 1.6 Volts.

[2] See Figure 1 and the 'Serial Interface' section.

[3] Common Mode Voltage.

[4] Mark/Space ratio for the SCLK input is 40/60 to 60/40.

[5] Measured with the load circuit of Figure 2 and defined as the time required for the output to cross 0.8 V or 2.4 V with V_{DD} = 5 V and time for an output to cross 0.4 V or 2.0 V for V_{DD} = 3 V.

[6] t_8 is derived from the measured time taken by the data outputs to change 0.5 V when loaded with the circuit of Figure 2. The measured number is then extrapolated back to remove the effects of charging or discharging the 50 pF capacitor. This means that the time, t_8, quoted in the timing characteristics is the true bus relinquish time of the part and is independent of the bus loading.

[7] See 'Power-up Time' Section.

Specifications subject to change without notice.

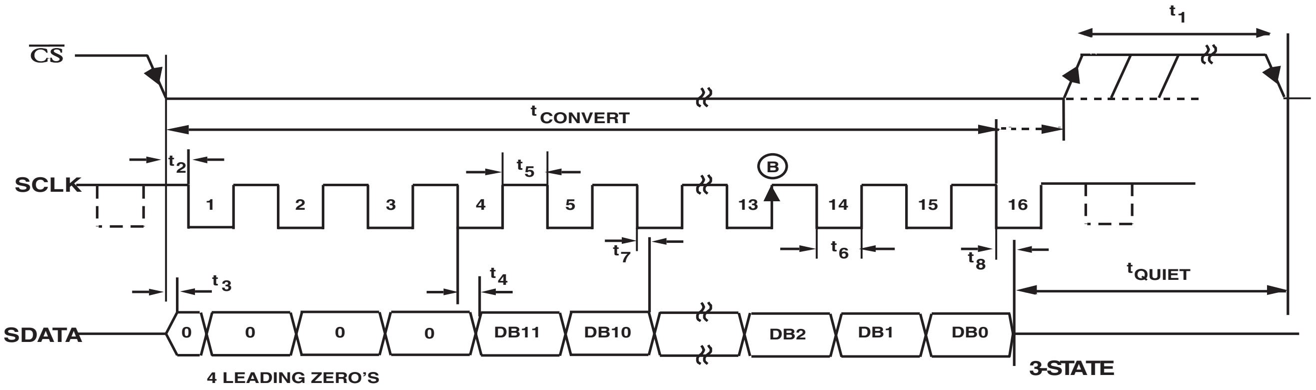


Figure 1. AD7452 Serial Interface Timing Diagram

ABSOLUTE MAXIMUM RATINGS[1]

(T_A = +25°C unless otherwise noted)

V_{DD} to GND	-0.3 V to +7 V
V_{IN+} to GND	–0.3 V to V_{DD} + 0.3 V
V_{IN-} to GND	–0.3 V to V_{DD} + 0.3 V
Digital Input Voltage to GND	-0.3 V to +7 V
Digital Output Voltage to GND	-0.3 V to V_{DD} + 0.3 V
V_{REF} to GND	-0.3 V to V_{DD} +0.3 V
Input Current to Any Pin Except Supplies[2]	±10mA
Operating Temperature Range	
Commercial (B Version)	-40°C to +85°C
Storage Temperature Range	-65°C to +150°C
Junction Temperature	+150°C
θ_{JA} Thermal Impedance	205.9°C/W (MSOP)
	211.5°C/W (SOT-23)
θ_{JC} Thermal Impedance	43.74°C/W (MSOP)
	91.99°C/W (SOT-23)
Lead Temperature, Soldering	
Vapor Phase (60 secs)	+215°C
Infared (15 secs)	+220°C
ESD	1kV

NOTES

[1] Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those listed in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

[2] Transient currents of up to 100 mA will not cause SCR latch up.

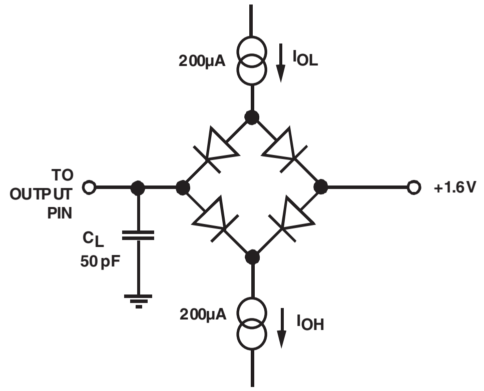


Figure 2. Load Circuit for Digital Output Timing Specifications

ORDERING GUIDE

Model	Range	Linearity Error (LSB)[1]	Package Option[4]	Branding Information
AD7452BRT	-40°C to +85°C	±1 LSB	RT-8	C07
AD7452BRM	-40°C to +85°C	±1 LSB	RM-8	C07
EVAL-AD7452CB	Evaluation Board			
EVAL-CONTROL BRD2[3]	Controller Board			

NOTES

[1] Linearity error here refers to Integral Non-linearity Error.

[2] This can be used as a stand-alone evaluation board or in conjunction with the EVALUATION BOARD CONTROLLER for evaluation/demonstration purposes.

[3] EVALUATION BOARD CONTROLLER. This board is a complete unit allowing a PC to control and communicate with all Analog Devices evaluation boards ending in the CB designators. To order a complete Evaluation Kit, you will need to order the ADC evaluation board i.e. EVAL-AD7452CB, the EVAL-CONTROL BRD2 and a 12V AC transformer. See the EVAL-AD7452CB technote for more information.

[4] RT = SOT-23; RM = MSOP

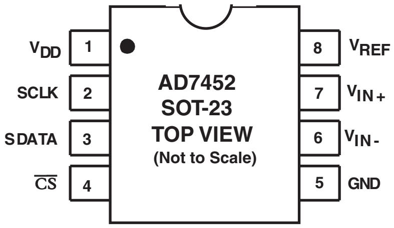
CAUTION

ESD (electrostatic discharge) sensitive device. Electrostatic charges as high as 4000 V readily accumulate on the human body and test equipment and can discharge without detection. Although the AD7452 features proprietary ESD protection circuitry, permanent damage may occur on devices subjected to high-energy electrostatic discharges. Therefore, proper ESD precautions are recommended to avoid performance degradation or loss of functionality.

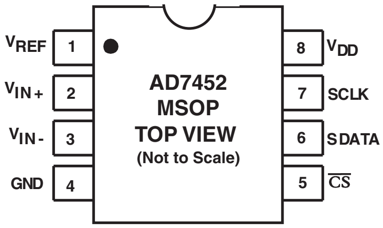
PIN FUNCTION DESCRIPTION

Pin Mnemonic	Function
V_{REF}	Reference Input for the AD7452. An external reference must be applied to this input. For a 5 V power supply, the reference is 2.5 V (±1%) and for a 3 V power supply, the reference is 2V (±1%) for specified performance. This pin should be decoupled to GND with a capacitor of at least 0.1µF. See the 'Reference Section' for more details.
V_{IN+}	Positive Terminal for Differential Analog Input.
V_{IN-}	Negative Terminal for Differential Analog Input.
GND	Analog Ground. Ground reference point for all circuitry on the AD7452. All analog input signals and any external reference signal should be referred to this GND voltage.
$\overline{CS}$	Chip Select. Active low logic input. This input provides the dual function of initiating a conversion on the AD7452 and framing the serial data transfer.
SDATA	Serial Data. Logic Output. The conversion result from the AD7452 is provided on this output as a serial data stream. The bits are clocked out on the falling edge of the SCLK input. The data stream of the AD7452 consists of four leading zeros followed by the 12 bits of conversion data which are provided MSB first. The output coding is two's complement.
SCLK	Serial Clock. Logic input. SCLK provides the serial clock for accessing data from the part. This clock input is also used as the clock source for the conversion process.
V_{DD}	Power Supply Input. V_{DD} is 3 V (+20%/-10%) or 5 V (±5%). This supply should be decoupled to GND with a 0.1µF Capacitor and a 10µF Tantalum Capacitor.

PIN CONFIGURATION 8-LEAD SOT-23



PIN CONFIGURATION 8-lead MSOP



TERMINOLOGY

Signal to (Noise + Distortion) Ratio
This is the measured ratio of signal to (noise + distortion) at the output of the ADC. The signal is the rms amplitude of the fundamental. Noise is the sum of all nonfundamental signals up to half the sampling frequency ($f_S/2$), excluding dc. The ratio is dependent on the number of quantization levels in the digitization process; the more levels, the smaller the quantization noise. The theoretical signal to (noise + distortion) ratio for an ideal N-bit converter with a sine wave input is given by:

$$\text{Signal to (Noise + Distortion)} = (6.02\,N + 1.76)\ dB$$

Thus for a 12-bit converter, this is 74 dB.

Total Harmonic Distortion
Total harmonic distortion (THD) is the ratio of the rms sum of harmonics to the fundamental. For the AD7452, it is defined as:

$$THD\ (dB) = 20\log\frac{\sqrt{V_2^2 + V_3^2 + V_4^2 + V_5^2 + V_6^2}}{V_1}$$

where V_1 is the rms amplitude of the fundamental and V_2, V_3, V_4, V_5 and V_6 are the rms amplitudes of the second to the sixth harmonics.

Peak Harmonic or Spurious Noise
Peak harmonic or spurious noise is defined as the ratio of the rms value of the next largest component in the ADC output spectrum (up to $f_S/2$ and excluding dc) to the rms value of the fundamental. Normally, the value of this specification is determined by the largest harmonic in the spectrum, but for ADCs where the harmonics are buried in the noise floor, it will be a noise peak.

Intermodulation Distortion
With inputs consisting of sine waves at two frequencies, fa and fb, any active device with nonlinearities will create distortion products at sum and difference frequencies of mfa ± nfb where m, n = 0, 1, 2, 3, etc. Intermodulation distortion terms are those for which neither m nor n are equal to zero. For example, the second order terms include (fa + fb) and (fa – fb), while the third order terms include (2fa + fb), (2fa – fb), (fa + 2fb) and (fa – 2fb).

The AD7452 is tested using the CCIF standard where two input frequencies near the top end of the input bandwidth are used. In this case, the second order terms are usually distanced in frequency from the original sine waves while the third order terms are usually at a frequency close to the input frequencies. As a result, the second and third order terms are specified separately. The calculation of the intermodulation distortion is as per the THD specification where it is the ratio of the rms sum of the individual distortion products to the rms amplitude of the sum of the fundamentals expressed in dBs.

Aperture Delay
This is the amount of time from the leading edge of the sampling clock until the ADC actually takes the sample.

Aperture Jitter
This is the sample to sample variation in the effective point in time at which the actual sample is taken.

Full Power Bandwidth
The full power bandwidth of an ADC is that input frequency at which the amplitude of the reconstructed fundamental is reduced by 0.1dB or 3dB for a full scale input.

Common Mode Rejection Ratio (CMRR)
The Common Mode Rejection Ratio is defined as the ratio of the power in the ADC output at full-scale frequency, f, to the power of a 100mV p-p sine wave applied to the Common Mode Voltage of V_{IN+} and V_{IN-} of frequency fs:

$$CMRR\ (dB) = 10\log(Pf/Pfs)$$

Pf is the power at the frequncy f in the ADC output; *Pfs* is the power at frequency fs in the ADC output.

Integral Nonlinearity (INL)
This is the maximum deviation from a straight line passing through the endpoints of the ADC transfer function.

Differential Nonlinearity (DNL)
This is the difference between the measured and the ideal 1 LSB change between any two adjacent codes in the ADC.

Zero Code Error
This is the deviation of the midscale code transition (111...111 to 000...000) from the ideal V_{IN+}-V_{IN-} (i.e., 0LSB).

Positive Gain Error
This is the deviation of the last code transition (011...110 to 011...111) from the ideal V_{IN+}-V_{IN-} (i.e., +V_{REF} - 1LSB), after the Zero Code Error has been adjusted out.

Negative Gain Error
This is the deviation of the first code transition (100...000 to 100...001) from the ideal V_{IN+}-V_{IN-} (i.e., -V_{REF} + 1LSB), after the Zero Code Error has been adjusted out.

Track/Hold Acquisition Time
The track/hold acquisition time is the minimum time required for the track and hold amplifier to remain in track mode for its output to reach and settle to within 0.5 LSB of the applied input signal.

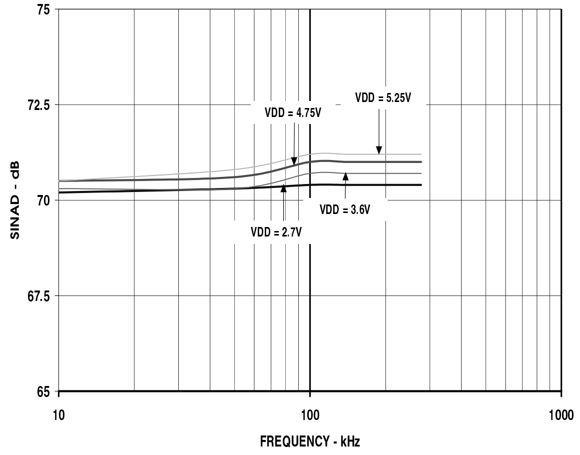
Power Supply Rejection Ratio (PSRR)
The power supply rejection ratio is defined as the ratio of the power in the ADC output at full-scale frequency, f, to the power of a 100mV p-p sine wave applied to the ADC V_{DD} supply of frequency fs. The frequency of this input varies from 1kHz to 1MHz.

$$PSRR\ (dB) = 10\log(Pf/Pfs)$$

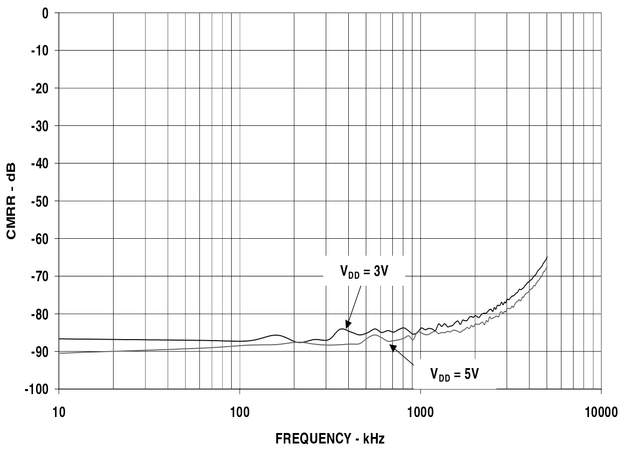
Pf is the power at frequency f in the ADC output; *Pfs* is the power at frequency fs in the ADC output.

PERFORMANCE CURVES

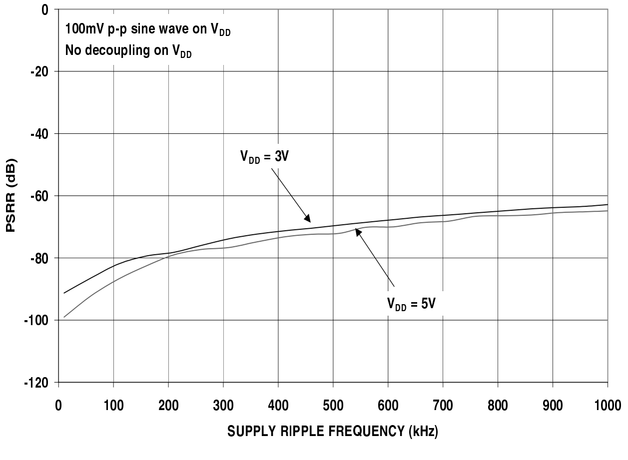
(Default Conditions: T_A = 25°C, F_S = 555kSPS, FSCLK = 10MHz)



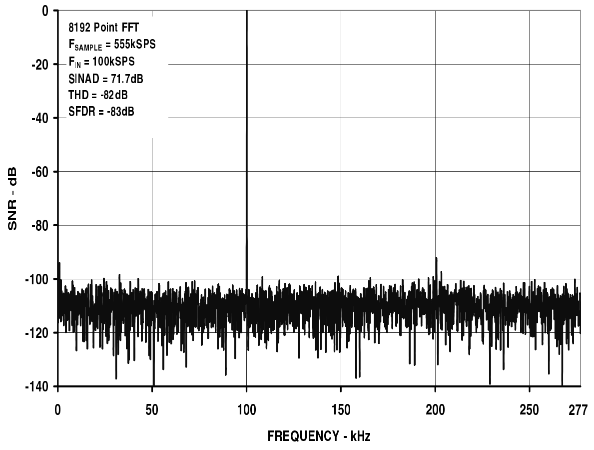
TPC 1. SINAD vs Analog Input Frequency for Various Supply Voltages



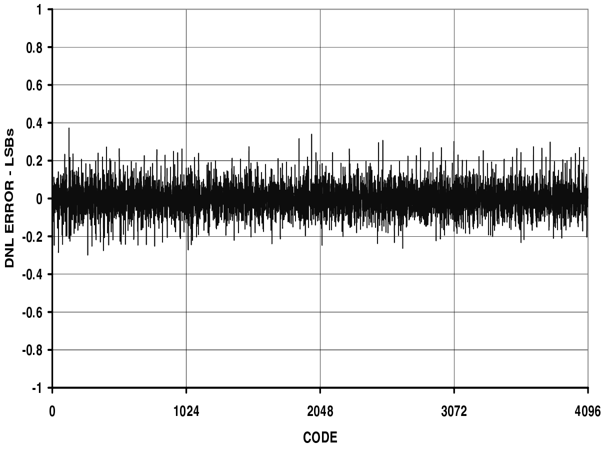
TPC 2. CMRR versus Frequency for V_{DD} = 5V and 3 V



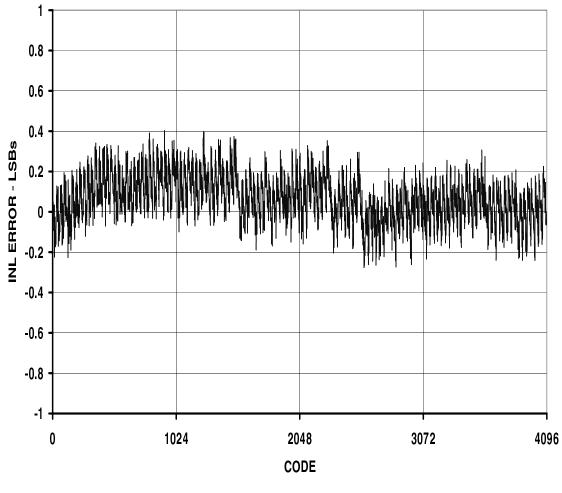
TPC 3. PSRR vs. Supply Ripple Frequency without Supply Decoupling



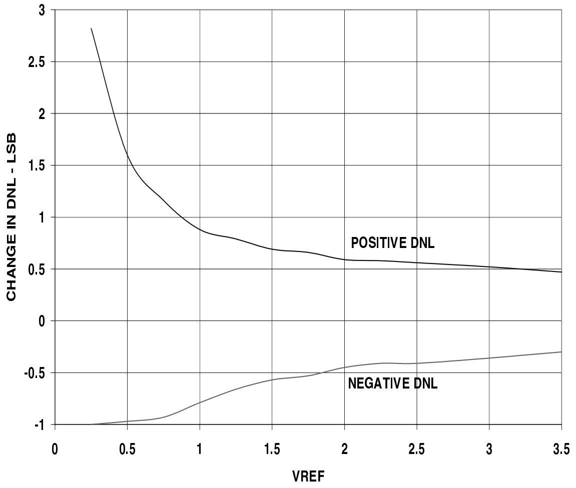
TPC 4. Dynamic Performance with V_{DD} =5V



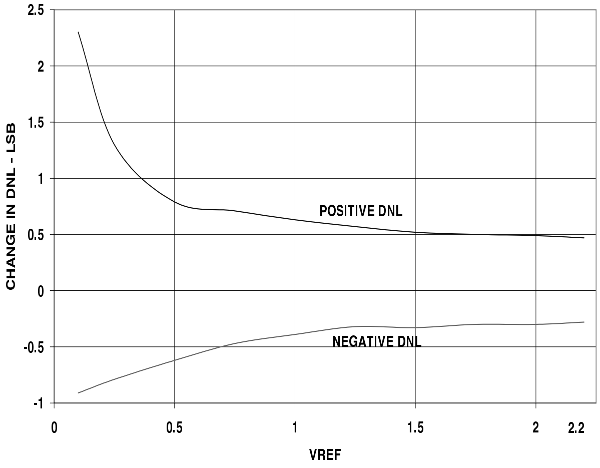
TPC 5. Typical DNL for V_{DD} = 5V



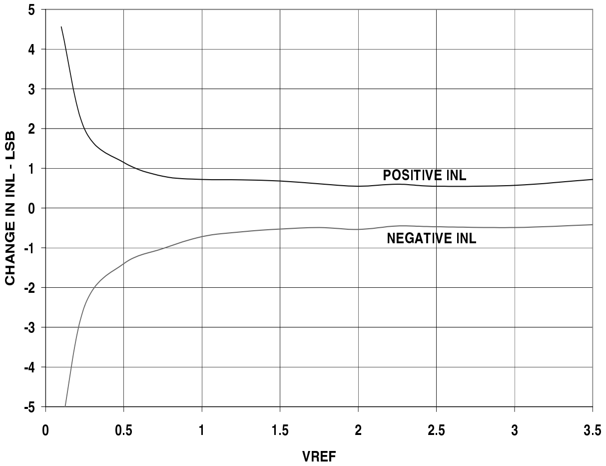
TPC 6. Typical INL for V_{DD} = 5V



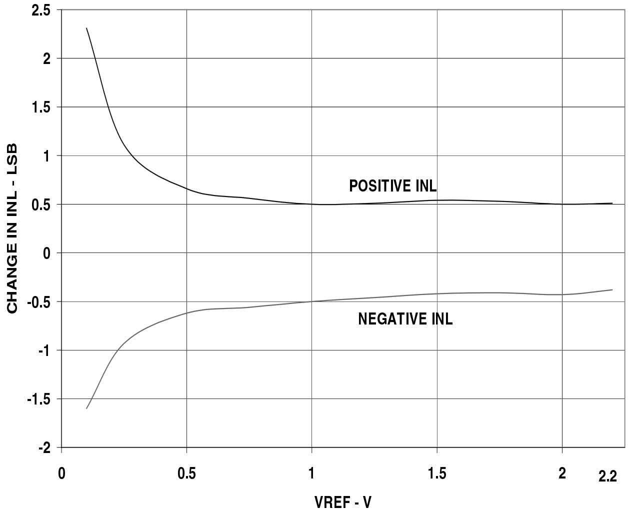
TPC 7. Change in DNL vs. V_{REF} for V_{DD} = 5V



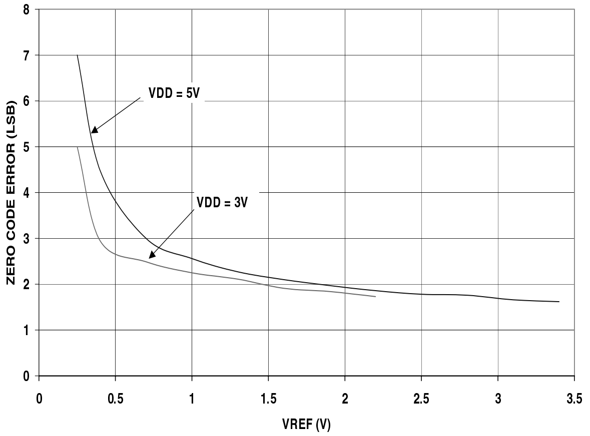
TPC 8. Change in DNL vs. V_{REF} for V_{DD} = 3 V



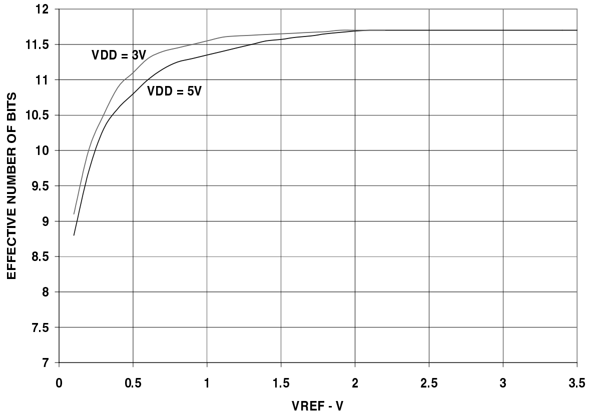
TPC 9. Change in INL vs. V_{REF} for V_{DD} = 5V



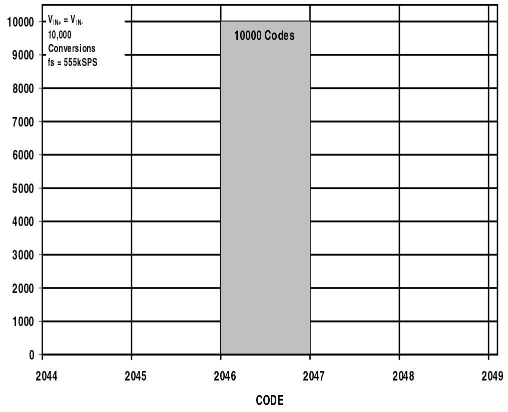
TPC 10. Change in INL vs. V_{REF} for V_{DD} = 3 V



TPC 11. Change in Zero Code Error vs Reference Voltage V_{DD} = 5V and 3 V



TPC 12.= Change in ENOB vs Reference Voltage V_{DD} = 5V and 3 V



TPC 13. Histogram of 10000 conversions of a DC Input with V_{DD} = 5V

CIRCUIT INFORMATION

The AD7452 is a low power, single supply, 12-bit successive approximation analog-to-digital converter (ADC). It can operate with a 5 V and 3V power supply and is capable of throughput rates up to 555kSPS when supplied with a 10MHz clock. It requires an external reference to be applied to the V_{REF} pin, with the value of the reference chosen depending on the power supply and what suits the application. When operated with a 5 V supply, the maximum reference that can be applied is 3.5 V and when operated with a 3 V supply, the maximum reference that can be applied is 2.2 V. (See 'Reference Section').The AD7452 has an on-chip differential track and hold amplifier, a successive approximation (SAR) ADC and a serial interface, housed in either an 8-lead SOT-23 or MSOP package. The serial clock input accesses data from the part and also provides the clock source for the successive-approximation ADC. The AD7452 features a power-down option for reduced power consumption between conversions. The power-down feature is implemented across the standard serial interface as described in the 'Modes of Operation' section.

CONVERTER OPERATION

The AD7452 is a successive approximation ADC based around two capacitive DACs. Figures 3 and 4 show simplified schematics of the ADC in Acquisition and Conversion phase respectively. The ADC comprises of Control Logic, a SAR and two capacitive DACs. In figure 3 (acquisition phase), SW3 is closed and SW1 and SW2 are in position A, the comparator is held in a balanced condition and the sampling capacitor arrays acquire the differential signal on the input.

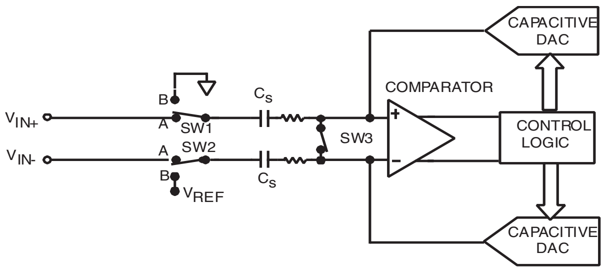


Figure 3. ADC Acquisition Phase

When the ADC starts a conversion (figure 4), SW3 will open and SW1 and SW2 will move to position B, causing the comparator to become unbalanced. Both inputs are disconnected once the conversion begins. The Control Logic and the charge redistribution DACs are used to add and subtract fixed amounts of charge from the sampling capacitor arrays to bring the comparator back into a balanced condition. When the comparator is rebalanced, the conversion is complete. The Control Logic generates the ADC's output code. The output impedances of the sources driving the V_{IN+} and the V_{IN-} pins must be matched otherwise the two inputs will have different settling times, resulting in errors.

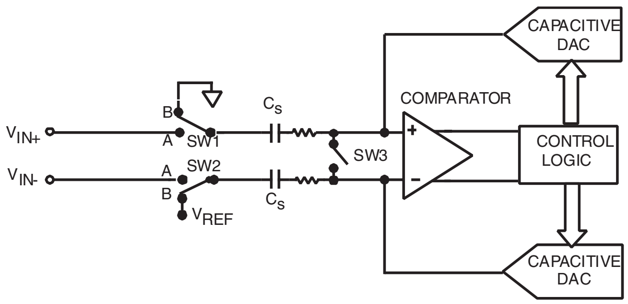


Figure 4. ADC Conversion Phase

ADC TRANSFER FUNCTION

The output coding for the AD7452 is two's complement. The designed code transitions occur at successive LSB values (i.e. 1LSB, 2LSBs, etc.). The LSB size of the AD7452 is $2xV_{REF}/4096$ and the ideal transfer characteristic is shown in figure 5.

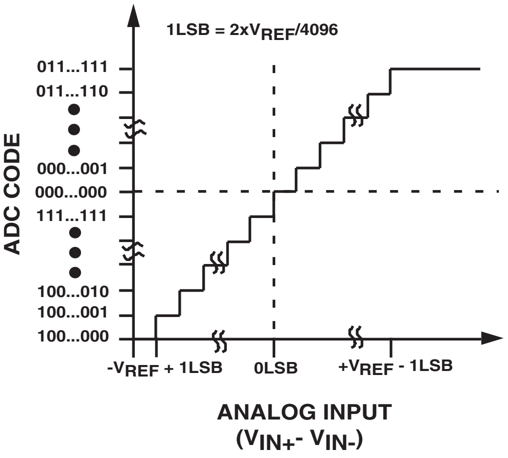


Figure 5. AD7452 Ideal Transfer Characteristic

TYPICAL CONNECTION DIAGRAM

Figure 6 shows a typical connection diagram for the AD7452 for both 5 V and 3 V supplies. In this setup the GND pin is connected to the analog ground plane of the system. The V_{REF} pin is connected to either a 2.5 V or a 2 V decoupled reference source depending on the power supply, to set up the analog input range. The common mode voltage has to be set up externally and is the value that the two inputs are centered on. The conversion result is output in a 16-bit word with four leading zeros followed by the MSB of the 12-bit result. For more details on driving the differential inputs and setting up the common mode, see the 'Driving Differential Inputs' section.

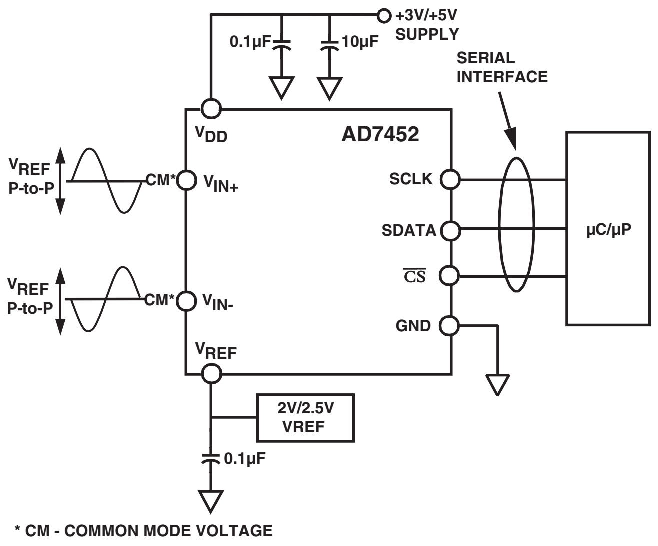


Figure 6. Typical Connection Diagram

THE ANALOG INPUT

The analog input of the AD7452 is fully differential. Differential signals have a number of benefits over single ended signals including noise immunity based on the device's common mode rejection, improvements in distortion performance, doubling of the device's available dynamic range and flexibility in input ranges and bias points. Figure 7 defines the fully differential analog input of the AD7452.

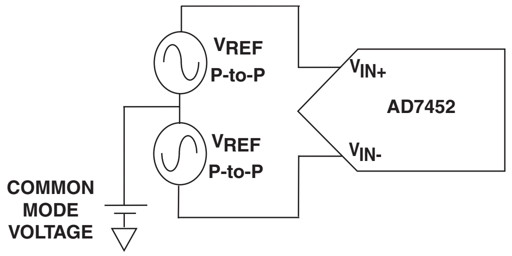


Figure 7. Differential Input Definition

The amplitude of the differential signal is the difference between the signals applied to the V_{IN+} and V_{IN-} pins (i.e. V_{IN+} - V_{IN-}). V_{IN+} and V_{IN-} are simultaneously driven by two signals each of amplitude V_{REF} that are 180° out of phase. The amplitude of the differential signal is therefore -V_{REF} to +V_{REF} peak-to-peak (i.e. 2 x V_{REF}). This is regardless of the common mode (CM). The common mode is the average of the two signals, i.e. $(V_{IN+} + V_{IN-})/2$ and is therefore the voltage that the two inputs are centered on. This results in the span of each input being CM ± $V_{REF}/2$. This voltage has to be set up externally and its range varies with V_{REF}. As the value of V_{REF} increases, the common mode range decreases. When driving the inputs with an amplfier, the actual common mode range will be determined by the amplifier's output voltage swing.

Figures 8 and 9 show how the common mode range typically varies with V_{REF} for both a 5 V and a 3 V power supply. The common mode must be in this range to guarantee the functionality of the AD7452.

For ease of use, the common mode can be set up to be equal to V_{REF}, resulting in the differential signal being ±V_{REF} centered on V_{REF}. When a conversion takes place, the common mode is rejected resulting in a virtually noise free signal of amplitude -V_{REF} to +V_{REF} corresponding to the digital codes of 0 to 4095.

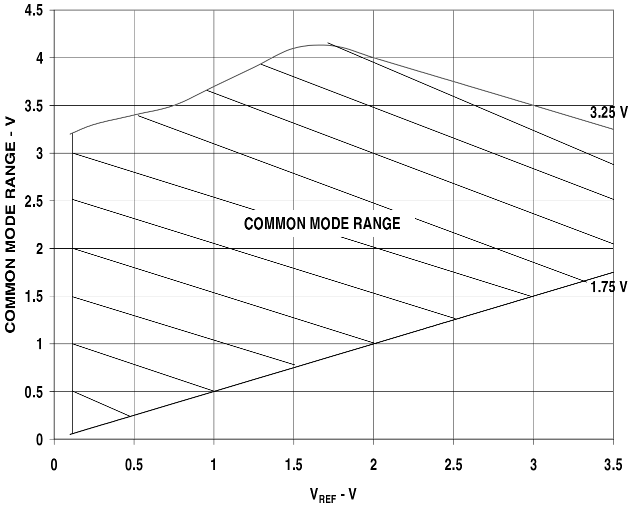


Figure 8. Input Common Mode Range versus V_{REF} (V_{DD} = 5V and V_{REF} (max) = 3.5V)

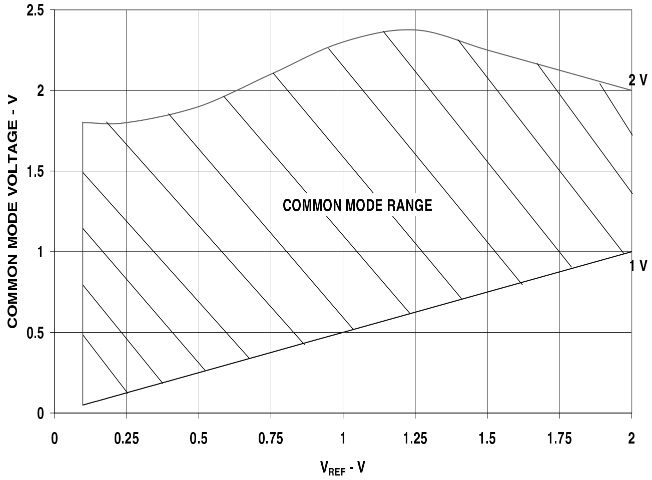


Figure 9. Input Common Mode Range versus V_{REF} (V_{DD}= 3V and V_{REF} (max) = 2V)

Figure 10 shows examples of the inputs to V_{IN+} and V_{IN-} for different values of V_{REF} for V_{DD} = 5 V. It also gives the maximum and minimum common mode voltages for each reference value according to figure 8.

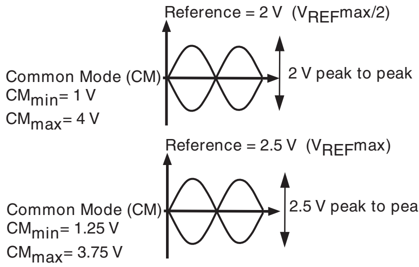


Figure 10. Examples of the Analog Inputs to V_{IN+} and V_{IN-} for Different Values of V_{REF} for V_{DD} = 5 V.

Analog Input Structure

Figure 11 shows the equivalent circuit of the analog input structure of the AD7452. The four diodes provide ESD protection for the analog inputs. Care must be taken to ensure that the analog input signals never exceed the supply rails by more than 300mV. This will cause these diodes to become forward biased and start conducting into the substrate. These diodes can conduct up to 10mA without causing irreversible damage to the part. The capacitors C1, in figure 11 are typically 4pF and can primarily be attributed to pin capacitance. The resistors are lumped components made up of the on-resistance of the switches. The value of these resistors is typically about 100Ω. The capacitors, C2, are the ADC's sampling capacitors and have a capacitance of 16pF typically.

For ac applications, removing high frequency components from the analog input signal is recommended by the use of an RC low-pass filter on the relevant analog input pins. In applications where harmonic distortion and signal to noise ratio are critical, the analog input should be driven from a low impedance source. Large source impedances will significantly affect the ac performance of the ADC. This may necessitate the use of an input buffer amplifier. The choice of the opamp will be a function of the particular application.

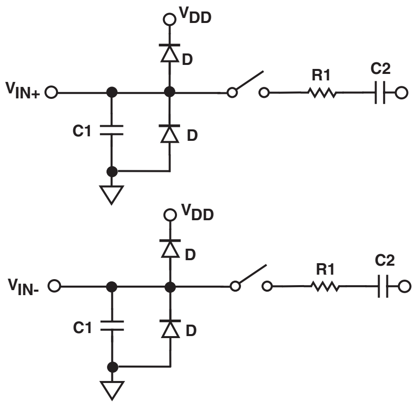


Figure 11. Equivalent Analog Input Circuit.
Conversion Phase - Switches Open
Track Phase - Switches Closed

When no amplifier is used to drive the analog input, the source impedance should be limited to low values. The maximum source impedance will depend on the amount of Total Harmonic Distortion (THD) that can be tolerated. The THD will increase as the source impedance increases and performance will degrade. Figure 12 shows a graph of the THD versus analog input signal frequency for different source impedances for both V_{DD} = 5 V and 3 V.

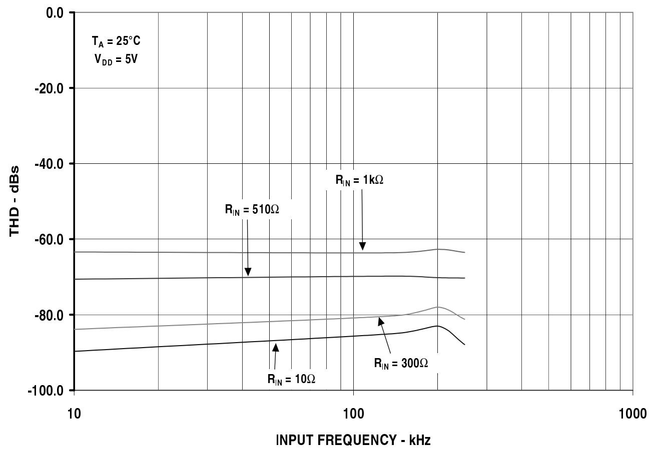


Figure 12. THD vs Analog Input Frequency for Various Source Impedances

Figure 13 shows a graph of THD versus analog input frequency for V_{DD} of 5 V ± 5% and 3 V +20%/-10%, while sampling at 555kSPS with a SCLK of 10 MHz. In this case the source impedance is 10Ω.

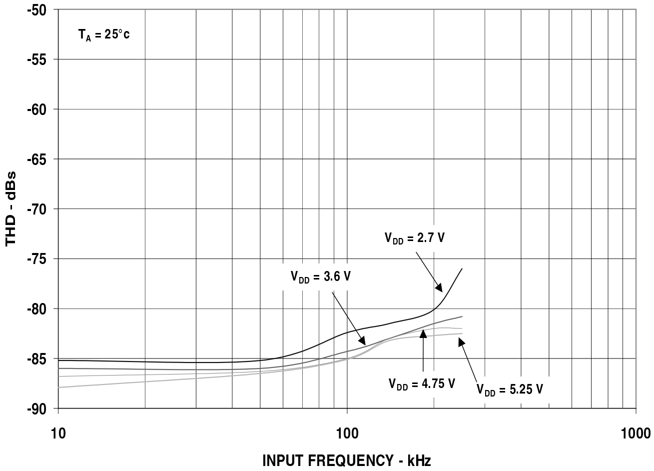


Figure 13. THD vs Analog Input Frequency for 3V and 5V Supply Voltages

DRIVING DIFFERENTIAL INPUTS

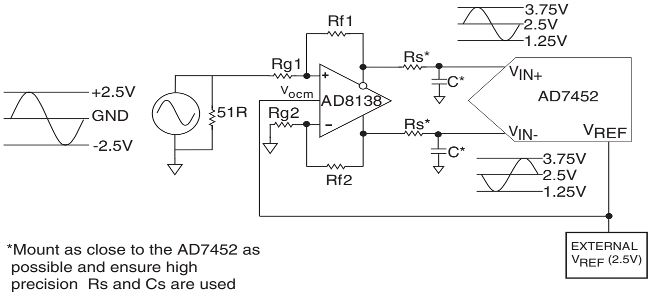
Differential operation requires that V_{IN+} and V_{IN-} be simultaneously driven with two equal signals that are 180° out of phase. The common mode must be set up externally and has a range which is determined by V_{REF}, the power supply and the particular amplifier used to drive the analog inputs (see figures 8 and 9). Differential modes of operation with either an ac or dc input, provide the best THD performance over a wide frequency range. Since not all applications have a signal preconditioned for differential operation, there is often a need to perform single ended to differential conversion.

Differential Amplifier

An ideal method of applying differential drive to the AD7452 is to use a differential amplifier such as the AD8138. This part can be used as a single ended to differential amplifier or as a differential to differential amplifier. In both cases the analog input needs to be bipolar. It also provides common mode level shifting and buffering of the bipolar input signal. Figure 14 shows how the AD8138 can be used as a single ended to differential amplifier. The positive and negative outputs of the AD8138 are connected to the respective inputs on the ADC via a pair of series resistors to minimize the effects of switched capacitance on the front end of the ADCs. The RC low pass filter on each analog input is recommended in ac applications to remove high frequency components of the analog input. The architecture of the AD8138 results in outputs that are very highly balanced over a wide frequency range without requiring tightly matched external components.

If the analog input source being used has zero impedance then all four resistors (Rg1, Rg2, Rf1, Rf2) should be the same. If the source has a 50 Ω impedance and a 50 Ω termination for example, the value of Rg2 should be increased by 25 Ω to balance this parallel impedance on the input and thus ensure that both the positive and negative analog inputs have the same gain (see figure 14). The outputs of the amplifier are perfectly matched, balanced differential outputs of identical amplitude and are exactly 180° out of phase.

The AD8138 is specified with 3 V, 5 V and ±5 V power supplies but the best results are obtained when it is supplied by ±5 V. A lower cost device that could also be used in this configuration with slight differences in characteristics to the AD8138 but with similar performance and operation is the AD8132.



*Mount as close to the AD7452 as possible and ensure high precision Rs and Cs are used

Rs - 50R; C - 1nF;
Rg1=Rf1=Rf2= 499R; Rg2 = 523R

Figure 14. Using the AD8138 as a Single Ended to Differential Amplifier

Opamp Pair

An opamp pair can be used to directly couple a differential signal to the AD7452. The circuit configurations shown in figures 15(a) and 15(b) show how a dual opamp can be used to convert a single ended signal into a differential signal for both a bipolar and a unipolar input signal respectively.

The voltage applied to point A sets up the Common Mode Voltage. In both diagrams, it is connected in some way to the reference but any value in the common mode range can be input here to setup the common mode. Examples of suitable dual opamps that could be used in this configuration to provide differential drive to the AD7452 are the TBD, TBD and the AD8022.

Care must be taken when chosing the opamp used, as the selection will depend on the required power supply and the system performance objectives. The driver circuits in figures 15(a) and 15(b) are optimized for dc coupling applications requiring optimum distortion performance. The differential op-amp driver circuit in figure 15(a) is configured to convert and level shift a single ended, ground referenced (bipolar) signal to a differential signal centered at the V_{REF} level of the ADC.

The circuit configuration shown in figure 15(b) converts a unipolar, single ended signal into a differential signal.

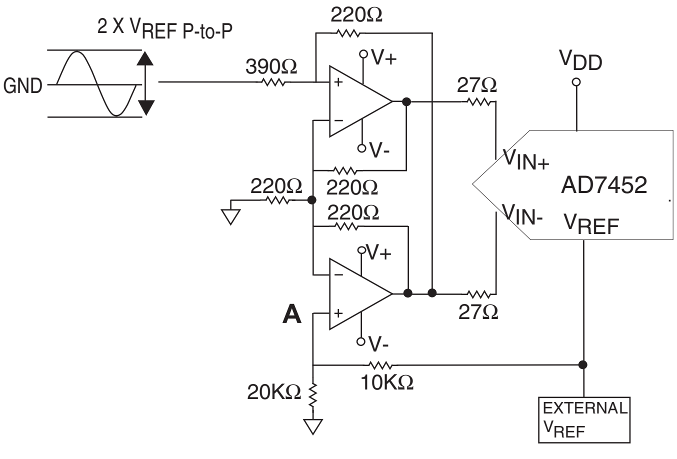


Figure 15 (a). Dual Opamp Circuit to Convert a Single Ended Bipolar Signal into a Differential Signal

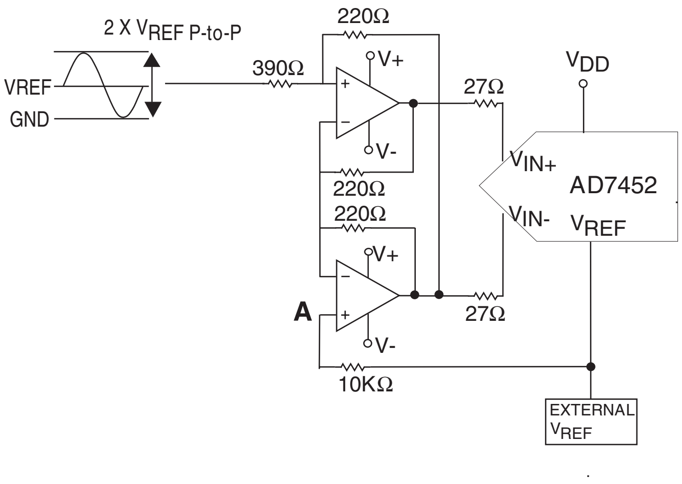


Figure 15(b). Dual Opamp Circuit to Convert a Single Ended Unipolar Signal into a Differential Signal

RF Transformer

In systems that do not need to be dc-coupled, an RF transformer with a center tap offers a good solution for generating differential inputs. Figure 16 shows how a transformer is used for single ended to differential conversion. It provides the benefits of operating the ADC in the differential mode without contributing additional noise and distortion. An RF transformer also has the benefit of providing electrical isolation between the signal source and the ADC. A transformer can be used for most ac applications. The center tap is used to shift the differential signal to the common mode level required, in this case it is connected to the reference so the common mode level is the value of the reference.

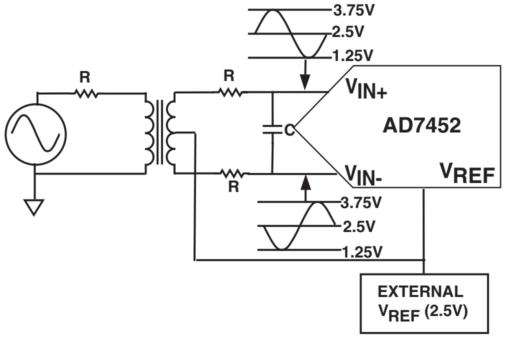


Figure 16. Using an RF Transformer to Generate Differential Inputs

REFERENCE SECTION

An external reference source is required to supply the reference to the AD7452. This reference input can range from 100 mV to 3.5 V. With a 5 V power supply, the specified reference is 2.5 V and maximum reference is 3.5 V. With a 3 V power supply, the specified reference is 2V and the maximum reference is 2.2 V. In both cases, the reference is functional from 100mV.

It is important to ensure that, when chosing the reference value for a particular application, the maximum analog input range (VINmax) is never greater than V_{DD} + 0.3V to comply with the maximum ratings of the device. The following two examples calculate the maximum V_{REF} input that can be used when operating the AD7452 at V_{DD} of 5 V and 3 V respectively.

Example 1:

$VINmax = V_{DD} + 0.3$

$VINmax = V_{REF} + V_{REF}/2$

If $V_{DD} = 5$ V

then $VINmax = 5.3$ V

Therefore $3xV_{REF}/2 = 5.3$ V

$\mathbf{V_{REF}\ max = 3.5\ V}$

Therefore, when operating at V_{DD} = 5 V, the value of V_{REF} can range from 100mV to a maximum value of 3.5V. When V_{DD} = 4.75 V, V_{REF} max = 3.17 V.

Example 2:

$VINmax = V_{DD} + 0.3$

$VINmax = V_{REF} + V_{REF}/2$

If $V_{DD} = 3V$

then $VINmax = 3.3$ V

Therefore $3xV_{REF}/2 = 3.3$ V

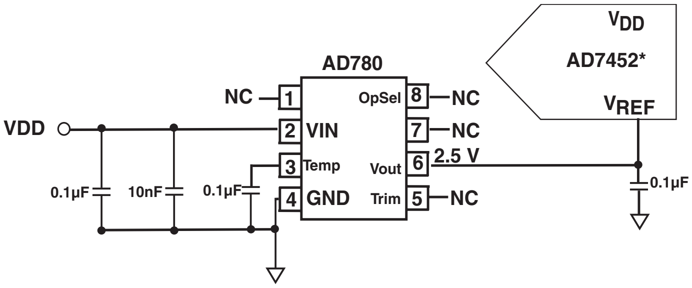
$\mathbf{V_{REF}\ max = 2.2\ V}$

Therefore, when operating at V_{DD} = 3 V, the value of V_{REF} can range from 100mV to a maximum value of 2.2V. When V_{DD} = 2.7 V, V_{REF} max = 2 V.

These examples show that the maximum reference applied to the AD7452 is directly dependant on the value applied to V_{DD}.

The value of the reference sets the analog input span and the common mode voltage range. Errors in the reference source will result in gain errors in the AD7452 transfer function and will add to specified full scale errors on the part. A capacitor of 0.1µF should be used to decouple the V_{REF} pin to GND.

Figure 17 shows a typical connection diagram for the V_{REF} pin. A recommended reference is the AD780.



*ADDITIONAL PINS OMITTED FOR CLARITY

Figure 17. Typical V_{REF} Connection Diagram

SINGLE ENDED OPERATION

When supplied with a 5 V power supply, the AD7452 can handle a single ended input. The design of this part is optimized for differential operation so with a single ended input, performance will degrade. Linearity will degrade by typically 0.2LSBs, the Full Scale Errors will degrade by typically 1LSBs and AC performance is not guaranteed.

To operate the AD7452 in single ended mode, the V_{IN+} input is coupled to the signal source while the V_{IN-} input is biased to the appropriate voltage corresponding to the mid-scale code transition. This voltage is the Common Mode, which is a fixed dc voltage (usually the reference). The V_{IN+} input swings around this value and should have voltage span of 2 x V_{REF} to make use of the full dynamic range of the part. The input signal will therefore have peak to peak values of Common Mode $\pm V_{REF}$. If the analog input is unipolar then an opamp in a non-inverting unity gain configuration can be used to drive the V_{IN+} pin. Because the ADC operates from a single supply, it will be necessary to level shift ground based bipolar signals to comply with the input requirements. An opamp can be configured to rescale and level shift the ground based bipolar signal so it is compatible with the selected input range of the AD7452 (see Figure 18).

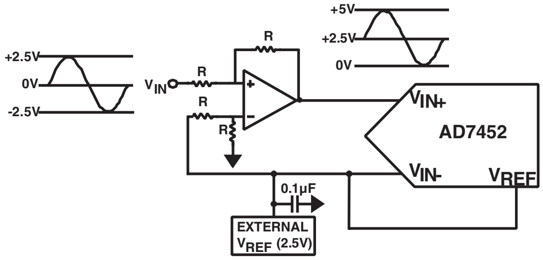


Figure 18. Applying a Bipolar Single Ended Input to the AD7452

SERIAL INTERFACE

Figures 1 shows a detailed timing diagram for the serial interface of the AD7452. The serial clock provides the conversion clock and also controls the transfer of data from the device during conversion. $\overline{CS}$ initiates the conversion process and frames the data transfer. The falling edge of $\overline{CS}$ puts the track and hold into hold mode and takes the bus out of three-state. The analog input is sampled and the conversion initiated at this point. The conversion will require 16 SCLK cycles to complete.

Once 13 SCLK falling edges have occurred, the track and hold will go back into track on the next SCLK rising edge as shown at point B in Figure 1. On the 16th SCLK falling edge the SDATA line will go back into three-state. If the rising edge of $\overline{CS}$ occurs before 16 SCLKs have elapsed, the conversion will be terminated and the SDATA line will go back into three-state on the 16th SCLK falling edge.

The conversion result from the AD7452 is provided on the SDATA output as a serial data streatm. The bits are clocked out on the falling edge of the SCLK input. The data stream of the AD7452 consists of four leading zeros, followed by 12 bits of conversion data which is provided MSB first. The output coding is twos complement. 16 serial clock cycles are required to perform a conversion and to access data from the AD7452. $\overline{CS}$ going low provides the first leading zero to be read in by the micro-controller or DSP. The remaining data is then clocked out on the subsequent SCLK falling edges beginning with the second leading zero. Thus the first falling clock edge on the serial clock provides the second leading zero. The final bit in the data transfer is valid on the 16th falling edge, having been clocked out on the previous (15th) falling edge.

Once the conversion is complete and the data has been accessed after the 16 clock cycles, it is important to ensure that, before the next conversion is initiated, enough time is left to meet the acquisition and quiet time specifications - see the Timing Example.

In applications with a slower SCLK, it may be possible to read in data on each SCLK rising edge i.e. the first rising edge of SCLK after the $\overline{CS}$ falling edge would have the leading zero provided and the 15th SCLK edge would have DB0 provided.

Timing Example

Having F_{SCLK} = 10MHz and a throughput rate of 555kSPS gives a cycle time of:

$1/\text{Throughput} = 1/555{,}000 = 1.8\mu s$

A cycle consists of:

$t_2 + 12.5\ (1/F_{SCLK}) + t_{ACQ} = 1.8\mu s.$

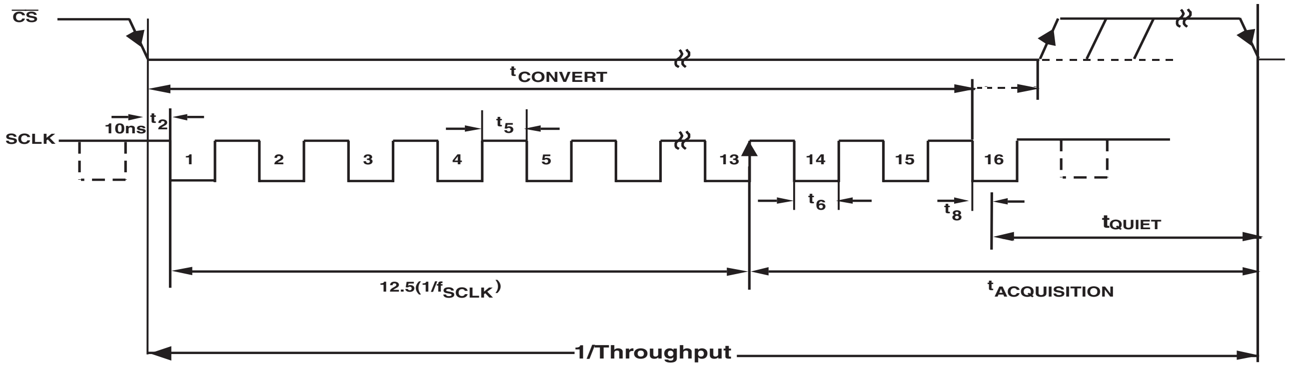


Figure 19. Serial Interface Timing Example

Therefore if t_2 = 10ns then:

10ns + 12.5(1/10MHz) + t_{ACQ} = 1µs

t_{ACQ} = 540ns

This 540ns satisfies the requirement of 290ns for t_{ACQ}.

From Figure 19, t_{ACQ} comprises of:

2.5(1/F_{SCLK}) + t_8 + t_{QUIET}

where t_8 = 35ns. This allows a value of 255ns for t_{QUIET} satisfying the minimum requirement of 60ns.

MODES OF OPERATION

The mode of operation of the AD7452 is selected by controlling the logic state of the $\overline{CS}$ signal during a conversion. There are two possible modes of operation, Normal Mode and Power-Down Mode. The point at which $\overline{CS}$ is pulled high after the conversion has been initiated will determine whether or not the AD7452 will enter the power-down mode. Similarly, if already in power-down, $\overline{CS}$ controls whether the devices will return to normal operation or remain in power-down. These modes of operation are designed to provide flexible power management options. These options can be chosen to optimize the power dissipation/throughput rate ratio for differing application requirements.

Normal Mode

This mode is intended for fastest throughput rate performance. The user does not have to worry about any power-up times with the AD7452 remaining fully powered up all the time. Figure 20 shows the general diagram of the operation of the AD7452 in this mode. The conversion is initiated on the falling edge of $\overline{CS}$ as described in the 'Serial Interface Section'. To ensure the part remains fully powered up, $\overline{CS}$ must remain low until at least 10 SCLK falling edges have elapsed after the falling edge of $\overline{CS}$.

If $\overline{CS}$ is brought high any time after the 10th SCLK falling edge, but before the 16th SCLK falling edge, the part will remain powered up but the conversion will be terminated and SDATA will go back into three-state. Sixteen serial clock cycles are required to complete the conversion and access the complete conversion result. $\overline{CS}$ may idle high until the next conversion or may idle low until sometime prior to the next conversion. Once a data transfer is complete, i.e. when SDATA has returned to three-state, another conversion can be initiated after the quiet time, t_{QUIET} has elapsed by again bringing $\overline{CS}$ low.

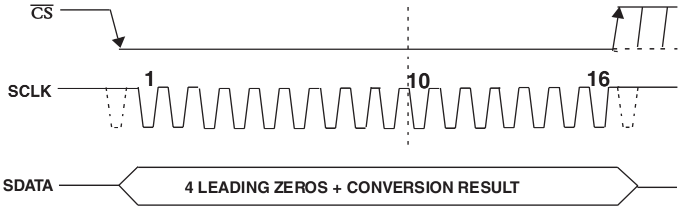


Figure 20. Normal Mode Operation

Power Down Mode

This mode is intended for use in applications where slower throughput rates are required; either the ADC is powered down between each conversion, or a series of conversions may be performed at a high throughput rate and the ADC is then powered down for a relatively long duration between these bursts of several conversions. When the AD7452 is in the power down mode, all analog circuitry is powered down. To enter power down mode, the conversion process must be interrupted by bringing $\overline{CS}$ high anywhere after the second falling edge of SCLK and before the tenth falling edge of SCLK as shown in Figure 21.

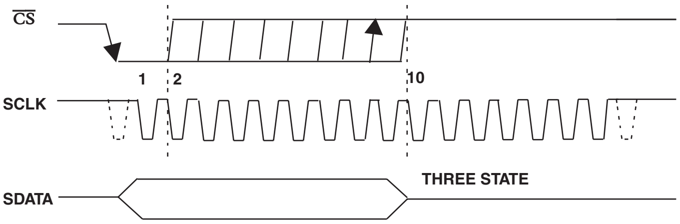


Figure 21. Entering Power Down Mode

Once $\overline{CS}$ has been brought high in this window of SCLKs, the part will enter power down and the conversion that was initiated by the falling edge of $\overline{CS}$ will be terminated and SDATA will go back into three-state. The time from the rising edge of $\overline{CS}$ to SDATA three-state enabled will never be greater than t_8 (see the 'Timing Specifications'). If $\overline{CS}$ is brought high before the second SCLK falling edge, the part will remain in normal mode and will not power-down. This will avoid accidental power-down due to glitches on the $\overline{CS}$ line.

In order to exit this mode of operation and power the AD7452 up again, a dummy conversion is performed. On the falling edge of $\overline{CS}$ the device will begin to power up, and will continue to power up as long as $\overline{CS}$ is held low until after the falling edge of the 10th SCLK. The device will be fully powered up after 1µsec has elapsed and, as shown in Figure 21, valid data will result from the next conversion.

If $\overline{CS}$ is brought high before the 10th falling edge of SCLK, the AD7452 will again go back into power-down. This avoids accidental power-up due to glitches on the $\overline{CS}$ line or an inadvertent burst of eight SCLK cycles while $\overline{CS}$ is low. So although the device may begin to power up on the falling edge of $\overline{CS}$, it will again power-down on the rising edge of $\overline{CS}$ as long as it occurs before the 10th SCLK falling edge.

Power up Time

The power up time of the AD7452 is typically 1µsec, which means that with any frequency of SCLK up to 10MHz, one dummy cycle (1.6µsec) will always be sufficient to allow the device to power-up. Once the dummy cycle is complete, the ADC will be fully powered up and the input signal will be acquired properly. The quiet time t_{QUIET} must still be allowed from the point at which the bus goes back into three-state after the dummy conversion, to the next falling edge of $\overline{CS}$.

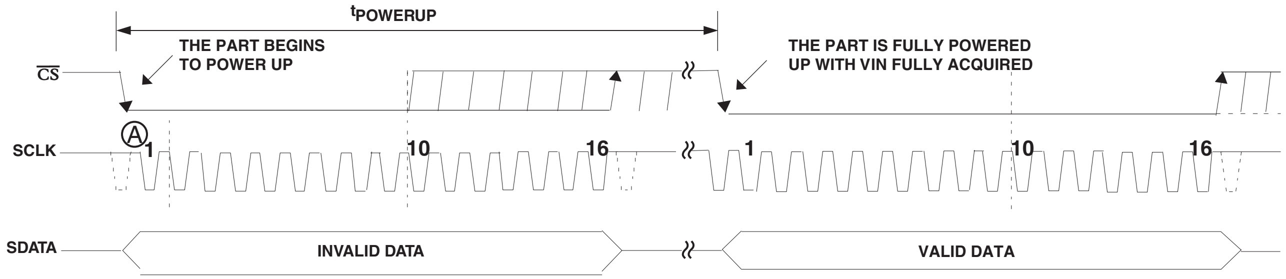


Figure 22. Exiting Power Down Mode

When running at the maximum throughput rate of 555kSPS, the AD7452 will power up and acquire a signal within ±0.5LSB in one dummy cycle. When powering up from the power-down mode with a dummy cycle, as in Figure 22, the track and hold, which was in hold mode while the part was powered down, returns to track mode after the first SCLK edge the part receives after the falling edge of $\overline{CS}$. This is shown as point A in Figure 22. Although at any SCLK frequency one dummy cycle is sufficient to power the device up and acquire V_{IN}, it does not necessarily mean that a full dummy cycle of 16 SCLKs must always elapse to power up the device and acquire V_{IN} fully; 1µs will be sufficient to power the device up and acquire the input signal.

For example, if a 5MHz SCLK frequency was applied to the ADC, the cycle time would be 3.2µs (i.e. 1/(5MHz) x 16). In one dummy cycle, 3.2µs, the part would be powered up and V_{IN} acquired fully. However after 1µs with a 5MHz SCLK only 5 SCLK cycles would have elapsed. At this stage, the ADC would be fully powered up and the signal acquired. So, in this case the $\overline{CS}$ can be brought high after the 10th SCLK falling edge and brought low again after a time t_{QUIET} to initiate the conversion.

When power supplies are first applied to the AD7452, the ADC may either power up in the power-down mode or normal mode. Because of this, it is best to allow a dummy cycle to elapse to ensure the part is fully powered up before attempting a valid conversion. Likewise, if the user wishes the part to power up in power-down mode, then the dummy cycle may be used to ensure the device is in power-down by executing a cycle such as that shown in Figure 21.

Once supplies are applied to the AD7452, the power up time is the same as that when powering up from the power-down mode. It takes approximately 1µs to power up fully if the part powers up in normal mode. It is not necessary to wait 1µs before executing a dummy cycle to ensure the desired mode of operation. Instead, the dummy cycle can occur directly after power is supplied to the ADC. If the first valid conversion is then performed directly after the dummy conversion, care must be taken to ensure that adequate acquisition time has been allowed. As mentioned earlier, when powering up from the power-down mode, the part will return to track upon the first SCLK edge applied after the falling edge of $\overline{CS}$. However, when the ADC powers up initially after supplies are applied, the track and hold will already be in track. This means if (assuming one has the facility to monitor the ADC supply current) the ADC powers up in the desired mode of operation and thus a dummy cycle is not required to change mode, then neither is a dummy cycle required to place the track and hold into track.

POWER VERSUS THROUGHPUT RATE

By using the power-down mode on the AD7452 when not converting, the average power consumption of the ADC decreases at lower throughput rates. Figure 23 shows how, as the throughput rate is reduced, the device remains in its power-down state longer and the average power consumption reduces accordingly. It shows this for both 5V and 3V power supplies.

For example, if the AD7452 is operated in continuous sampling mode with a throughput rate of 100kSPS and an SCLK of 10MHz and the device is placed in the power down mode between conversions, then the power consumption is calculated as follows:

Power dissipation during normal operation = 7.25 mW max (for V_{DD} = 5V).

If the power up time is 1 dummy cycle (1.06µsec if $\overline{CS}$ is brought high after the 10th SCLK falling edge and the brought low after the quiet time), and the remaining conversion time is another cycle i.e. 1.6µsec, then then AD7452 can be said to dissipate 7.25mW for 2.66µsec* during each conversion cycle.

If the throughput rate = 100kSPS then the cycle time = 10µsec and the average power dissipated during each cycle is:

(2.66/10) x 7.25mW = 1.92mW

For the same scenario, if V_{DD} = 3V, the power dissipation during normal operation is 3.3mW max.

The AD7452 can now be said to dissipate 3.3mW for 2.66µsec* during each conversion cycle.

The average power dissipated during each cycle with a throughput rate of 100kSPS is therefore:

(2.66/10) x 3.3mW = 0.88mW

This is how the power numbers in Figure 23 are calculated.

*This figure assumes a very short time used to enter the power down mode. This will increase as the burst of clocks used to enter the power down mode is increased.

For throughput rates above 320kSPS, it is recommended that for optimum power performance, the serial clock frequency is reduced.

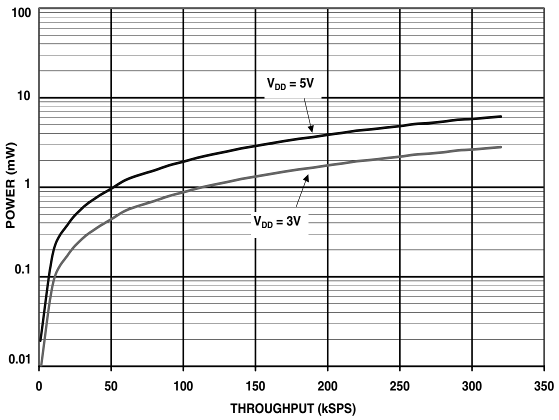


Figure 23. Power versus Throughput Rate for Power Down Mode

MICROPROCESSOR AND DSP INTERFACING

The serial interface on the AD7452 allows the part to be directly connected to a range of different microprocessors. This section explains how to interface the AD7452 with some of the more common microcontroller and DSP serial interface protocols.

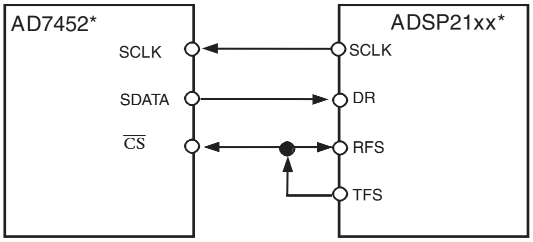
AD7452 to ADSP21xx

The ADSP21xx family of DSPs are interfaced directly to the AD7452 without any glue logic required.

The SPORT control register should be set up as follows:
TFSW = RFSW = 1, Alternate Framing
INVRFS = INVTFS = 1, Active Low Frame Signal
DTYPE = 00, Right Justify Data
SLEN = 1111, 16-Bit Data words
ISCLK = 1, Internal serial clock
TFSR = RFSR = 1, Frame every word
IRFS = 0,
ITFS = 1.

To implement the power-down mode SLEN should be set to 1001 to issue an 8-bit SCLK burst.

The connection diagram is shown in Figure 24. The ADSP21xx has the TFS and RFS of the SPORT tied together, with TFS set as an output and RFS set as an input. The DSP operates in Alternate Framing Mode and the SPORT control register is set up as described. The Frame Synchronisation signal generated on the TFS is tied to $\overline{CS}$ and as with all signal processing applications equidistant sampling is necessary. However, in this example, the timer interrupt is used to control the sampling rate of the ADC and under certain conditions, equidistant sampling may not be acheived.



*ADDITIONAL PINS OMITTED FOR CLARITY

Figure 24. Interfacing to the ADSP 21xx

The timer registers etc., are loaded with a value which will provide an interrupt at the required sample interval. When an interrupt is received, a value is transmitted with TFS/DT (ADC control word). The TFS is used to control the RFS and hence the reading of data. The frequency of the serial clock is set in the SCLKDIV register. When the instruction to transmit with TFS is given, (i.e. AX0=TX0), the state of the SCLK is checked. The DSP will wait until the SCLK has gone High, Low and High before transmission will start. If the timer and SCLK values are chosen such that the instruction to transmit occurs on or near the rising edge of SCLK, then the data may be transmitted or it may wait until the next clock edge.

For example, the ADSP-2111 has a master clock frequency of 16MHz. If the SCLKDIV register is loaded with the value 3 then a SCLK of 2MHz is obtained, and 8 master clock periods will elapse for every 1 SCLK period. If the timer registers are loaded with the value 803, then 100.5 SCLKs will occur between interrupts and subsequently between transmit instructions. This situation will result in non-equidistant sampling as the transmit instruction is occuring on a SCLK edge. If the number of SCLKs between interrupts is a whole integer figure of N then equidistant sampling will be implemented by the DSP.

AD7452 to TMS320C5x/C54x

The serial interface on the TMS320C5x/C54x uses a continuous serial clock and frame synchronization signals to synchronize the data transfer operations with peripheral devices like the AD7452. The $\overline{CS}$ input allows easy interfacing between the TMS320C5x/C54x and the AD7452 without any glue logic required. The serial port of the TMS320C5x/C54x is set up to operate in burst mode with internal CLKX (TX serial clock) and FSX (TX frame sync). The serial port control register (SPC) must have the following setup: FO = 0, FSM = 1, MCM = 1 and TXM = 1. The format bit, FO, may be set to 1 to set the word length to 8-bits, in order to implement the power-down mode on the AD7452. The connection diagram is shown in Figure 25. It should be noted that for signal processing applications, it is imperative that the frame synchronisation signal from the TMS320C5x/C54x will provide equidistant sampling.

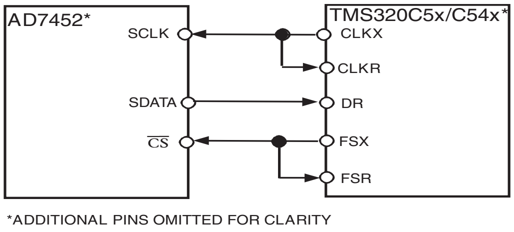


Figure 25. Interfacing to the TMS320C5x/C54x

AD7452 to DSP56xxx

The connection diagram in figure 26 shows how the AD7452 can be connected to the SSI (Synchronous Serial Interface) of the DSP56xxx family of DSPs from Motorola. The SSI is operated in Synchronous Mode (SYN bit in CRB =1) with internally generated 1-bit clock period frame sync for both Tx and Rx (bits FSL1 =1 and FSL0 =0 in CRB). Set the word length to 16 by setting bits WL1 =1 and WL0 = 0 in CRA. To implement the power-down mode on the AD7452 then the word length can be changed to 8 bits by setting bits WL1 = 0 and WL0 = 0 in CRA. It should be noted that for signal processing applications, it is imperative that the frame synchronisation signal from the DSP56xxx will provideequidistant sampling.

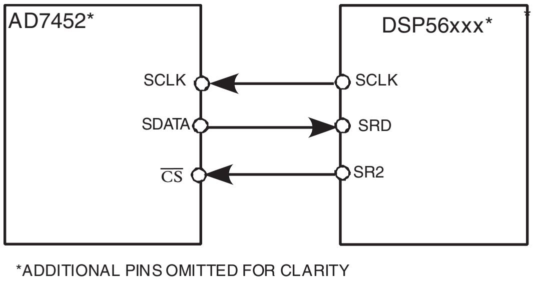


Figure 26. Interfacing to the DSP56xx

APPLICATION HINTS

Grounding and Layout

The printed circuit board that houses the AD7452 should be designed so that the analog and digital sections are separated and confined to certain areas of the board. This facilitates the use of ground planes that can be easily separated. A minimum etch technique is generally best for ground planes as it gives the best shielding. Digital and analog ground planes should be joined in only one place and the connection should be a star ground point established as close to the GND pin on the AD7452 as possible. Avoid running digital lines under the device as this will couple noise onto the die. The analog ground plane should be allowed to run under the AD7452 to avoid noise coupling. The power supply lines to the AD7452 should use as large a trace as possible to provide low impedance paths and reduce the effects of glitches on the power supply line.

Fast switching signals like clocks should be shielded with digital ground to avoid radiating noise to other sections of the board, and clock signals should never run near the analog inputs. Avoid crossover of digital and analog signals. Traces on opposite sides of the board should run at right angles to each other. This will reduce the effects of feedthrough through the board. A microstrip technique is by far the best but is not always possible with a double-sided board.

In this technique the component side of the board is dedicated to ground planes while signals are placed on the solder side.

Good decoupling is also important. All analog supplies should be decoupled with 10µF tantalum capacitors in parallel with 0.1µF capacitors to GND. To achieve the best from these decoupling components, they must be placed as close as possible to the device.

EVALUATING THE AD7452 PERFORMANCE

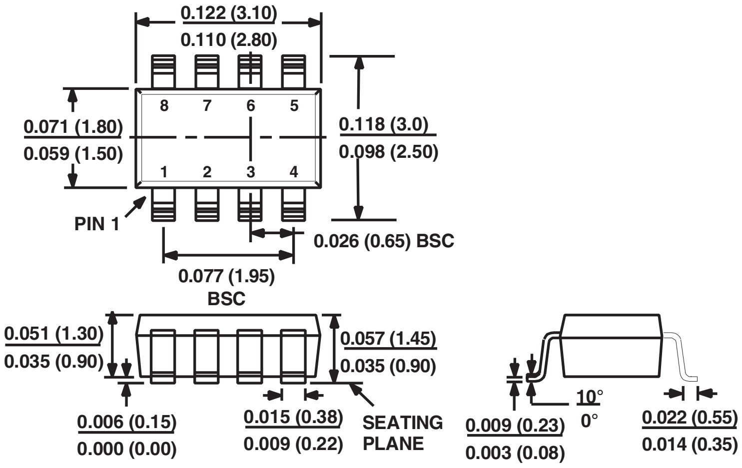
An evaluation board is available for the AD7452. The evaluation board package includes a fully assembled and tested evaluation board, documentation and software for controlling the board from a PC via the Evaluation Board Controller. The Evaluation Board Controller can be used in conjunction with the AD7452 Evaluation board as well as many other Analog Devices evaluation boards ending with the CB designator, to demonstrate/evaluate the ac and dc performance of the AD7452.

The software allows the user to perform ac (fast Fourier Transform) and dc (Histogram of codes) tests on the AD7452. See the evaluation board technical note for more information.

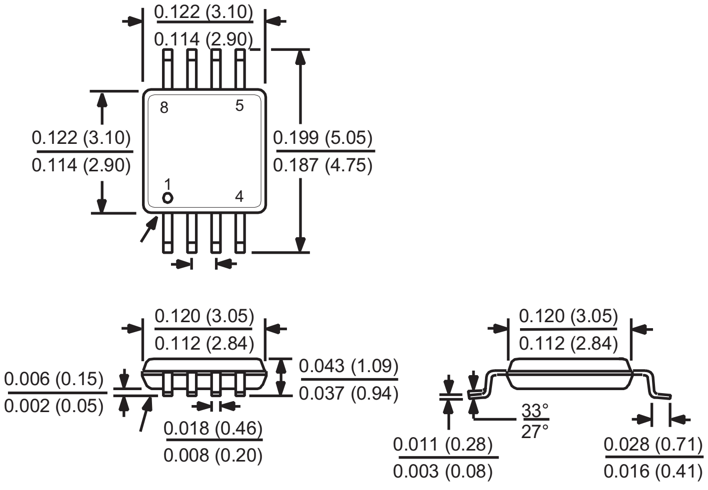
OUTLINE DIMENSIONS

Dimensions shown in inches (millimeters)

8-LEAD SOT-23 (RT-8)



8-LEAD MSOP (RM-8)



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