![ANALOG DEVICES]

Audio/Video 60 MHz 16 × 16, G = +2 Crosspoint Switch

AD8113

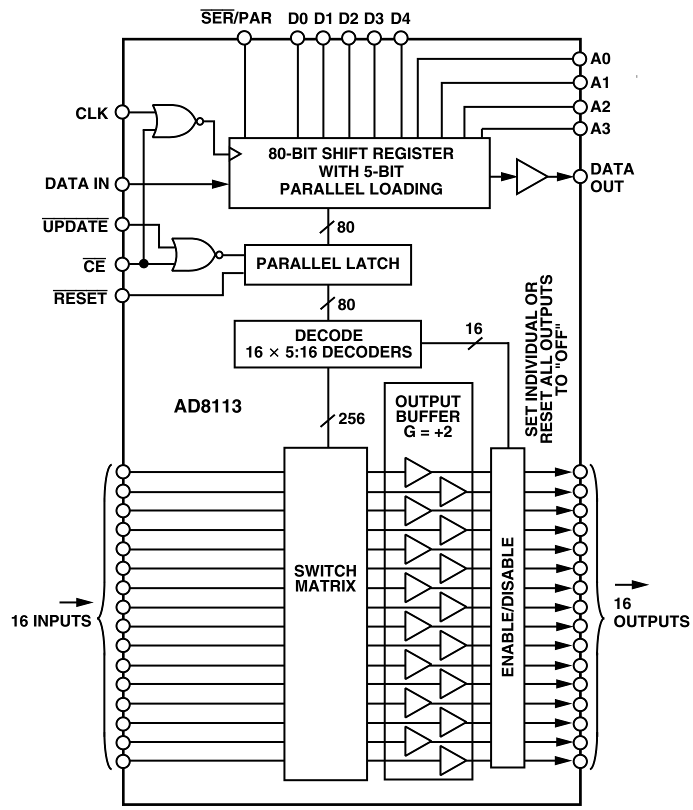
FEATURES

- 16 × 16 High Speed Nonblocking Switch Array
- Serial or Parallel Programming of Switch Array
- Serial Data Out Allows Daisy Chaining Control of Multiple 16 × 16s to Create Larger Switch Arrays
- Output Disable Allows Connection of Multiple Devices without Loading the Output Bus
- Complete Solution
  - Buffered Inputs
  - 16 Output Amplifiers
  - Operates on ±5 V or ±12 V Supplies
  - Low Supply Current of 54 mA
- Excellent Audio Performance V_S = ±12 V
  - ±10 V Output Swing
  - 0.002% THD @ 20 kHz Max. 20 V p-p (R_L = 600 Ω)
- Excellent Video Performance V_S = ±5 V
  - 10 MHz 0.1 dB Gain Flatness
  - 0.1% Differential Gain Error (R_L = 1 kΩ)
  - 0.1° Differential Phase Error (R_L = 1 kΩ)
- Excellent AC Performance
  - –3 dB Bandwidth 60 MHz
- Low All Hostile Crosstalk of
  - –83 dB @ 20 kHz
- Reset Pin Allows Disabling of All Outputs (Connected to a Capacitor to Ground Provides Power-On Reset Capability)
- 100-Lead LQFP (14 mm × 14 mm)

APPLICATIONS

- Analog/Digital Audio Routers
- Video Routers (NTSC, PAL, S-VIDEO, SECAM)
- Multimedia Systems
- Video Conferencing
- CCTV Surveillance

FUNCTIONAL BLOCK DIAGRAM



PRODUCT DESCRIPTION

The AD8113 is a fully buffered crosspoint switch matrix that operates on ±12 V for audio applications and ±5 V for video applications. It offers a –3 dB signal bandwidth greater than 60 MHz and channel switch times of less than 60 ns with 0.1% settling for use in both analog and digital audio. The AD8113 operated at 20 kHz has crosstalk performance of –83 dB and isolation of 90 dB. In addition, ground/power pins surround all inputs and outputs to provide extra shielding for operation in the most demanding audio routing applications. The differential gain and differential phase of better than 0.1% and 0.1°, respectively, along with 0.1 dB flatness out to 10 MHz, make the AD8113 suitable for many video applications.

The AD8113 includes 16 independent output buffers that can be placed into a disabled state for paralleling crosspoint outputs so that off channel loading is minimized. The AD8113 has a gain of +2. It operates on voltage supplies of ±5 V or ±12 V while consuming only 34 mA or 31 mA of current, respectively. The channel switching is performed via a serial digital control (which can accommodate daisy-chaining of several devices) or via a parallel control, allowing updating of an individual output without reprogramming the entire array.

The AD8113 is packaged in a 100-lead LQFP and is available over the commercial temperature range of 0°C to 70°C.

REV. A

One Technology Way, P.O. Box 9106, Norwood, MA 02062-9106, U.S.A.
Tel: 781/329-4700 www.analog.com
Fax: 781/326-8703

AD8113–SPECIFICATIONS (T_A = 25°C, V_S = ±12 V, R_L = 600 Ω, unless otherwise noted.)

Parameter	Conditions	Min	Typ	Max	Unit
DYNAMIC PERFORMANCE					
–3 dB Bandwidth	V_{OUT} = 200 mV p-p, R_L = 600 Ω, V_S = ±12 V	46	60		MHz
	V_{OUT} = 200 mV p-p, R_L = 150 Ω, V_S = ±5 V	41	60		MHz
	V_{OUT} = 8 V p-p, R_L = 600 Ω, V_S = ±12 V		10		MHz
	V_{OUT} = 2 V p-p, R_L = 150 Ω, V_S = ±5 V		25		MHz
Gain Flatness	0.1 dB, V_{OUT} = 200 mV p-p, R_L =150 Ω, V_S = ±5 V		10		MHz
Propagation Delay	V_{OUT} = 2 V p-p, R_L = 150 Ω		20		ns
Settling Time	0.1%, 2 V Step, R_L =150 Ω, V_S = ±5 V		23		ns
Slew Rate	2 V Step, R_L =150 Ω, V_S = ±5 V		100		V/µs
	20 V Step, R_L =600 Ω, V_S = ±12 V		120		V/µs
NOISE/DISTORTION PERFORMANCE					
Differential Gain Error	NTSC, R_L = 1 kΩ, V_S = ±5 V		0.1		%
Differential Phase Error	NTSC, R_L = 1 kΩ, V_S = ±5 V		0.1		Degrees
Total Harmonic Distortion	20 kHz, R_L = 600 Ω, 20 V p-p		0.002		%
Crosstalk, All Hostile	f = 5 MHz, R_L =150 Ω, V_S = ±5 V		–67		dB
	f = 20 kHz		–83		dB
Off Isolation	f = 5 MHz, R_L =150 Ω, V_S = ±5 V, One Channel		–100		dB
	f = 20 kHz, One Channel		–83		dB
Input Voltage Noise	20 kHz		14		$nV/\sqrt{Hz}$
	0.1 MHz–10 MHz		12		$nV/\sqrt{Hz}$
DC PERFORMANCE					
Gain Error	No Load, V_S = ±12 V, V_{OUT} = ±8 V		0.3	2.5	%
	R_L = 600 Ω, V_S = ±12 V		0.5		%
	R_L = 150 Ω, V_S = ±5 V		0.5		%
Gain Matching	No Load, Channel-to-Channel		0.7	3.5	%
	R_L = 600 Ω, Channel-to-Channel		0.7		%
	R_L = 150 Ω, Channel-to-Channel		0.7		%
Gain Temperature Coefficient			20		ppm/°C
OUTPUT CHARACTERISTICS					
Output Resistance	Enabled		0.3		Ω
	Disabled	3.4	4		kΩ
Output Capacitance	Disabled		5		pF
Output Voltage Swing	V_S = ±5 V, No Load	±3.2	±3.5		V
	V_S = ±12 V, No Load	±10.3	±10.5		V
	I_{OUT} = 20 mA, V_S = ±5 V	±2.7	±3		V
	I_{OUT} = 20 mA, V_S = ±12 V	±9.8	±10		V
Short Circuit Current	R_L = 0 Ω		55		mA
INPUT CHARACTERISTICS					
Input Offset Voltage	All Configurations		±4.5	±8.5	mV
	Temperature Coefficient		10		µV/°C
Input Voltage Range	No Load, V_S = ±5 V		±1.5		V
	V_S = ±12 V		±5.0		V
Input Capacitance	Any Switch Configuration		4		pF
Input Resistance			50		MΩ
Input Bias Current	Any Number of Enabled Inputs		1	±1.6	µA
SWITCHING CHARACTERISTICS					
Enable On Time			80		ns
Switching Time, 2 V Step	50% Update to 1% Settling		50		ns
Switching Transient (Glitch)			20		mV p-p
POWER SUPPLIES					
Supply Current	AV_{CC} Outputs Enabled, No Load, V_S = ±12 V		50	54	mA
	AV_{CC} Outputs Disabled, V_S = ±12 V		34	38	mA
	AV_{CC} Outputs Enabled, No Load, V_S = ±5 V		45	50	mA
	AV_{CC} Outputs Disabled, V_S = ±5 V		31	35	mA
	AV_{EE} Outputs Enabled, No Load, V_S = ±12 V		50	54	mA
	AV_{EE} Outputs Disabled, V_S = ±12 V		34	38	mA
	AV_{EE} Outputs Enabled, No Load, V_S = ±5 V		45	50	mA
	AV_{EE} Outputs Disabled, V_S = ±5 V		31	35	mA
	DV_{CC} Outputs Enabled, No Load		8	13	mA

Parameter	Conditions	Min	Typ	Max	Unit
DYNAMIC PERFORMANCE					
Supply Voltage Range	AV_{CC}	4.5		12.6	V
	AV_{EE}	–12.6		–4.5	V
	DV_{CC}	4.5		5.5	V
PSRR	DC	75	80		dB
	f = 100 kHz		60		dB
	f = 1 MHz		40		dB
OPERATING TEMPERATURE RANGE					
Temperature Range	Operating (Still Air)		0 to 70		°C
θ_{JA}	Operating (Still Air)		40		°C/W

Specifications subject to change without notice.

TIMING CHARACTERISTICS (Serial)

Parameter	Symbol	Limit Min	Typ	Max	Unit
Serial Data Setup Time	t_1	20			ns
CLK Pulsewidth	t_2	100			ns
Serial Data Hold Time	t_3	20			ns
CLK Pulse Separation, Serial Mode	t_4	100			ns
CLK to $\overline{\text{UPDATE}}$ Delay	t_5	0			ns
$\overline{\text{UPDATE}}$ Pulsewidth	t_6	50			ns
CLK to DATA OUT Valid, Serial Mode	t_7			200	ns
Propagation Delay, $\overline{\text{UPDATE}}$ to Switch On or Off				50	ns
Data Load Time, CLK = 5 MHz, Serial Mode			16		µs
CLK, $\overline{\text{UPDATE}}$ Rise and Fall Times				100	ns
$\overline{\text{RESET}}$ Time				200	ns

Specifications subject to change without notice.

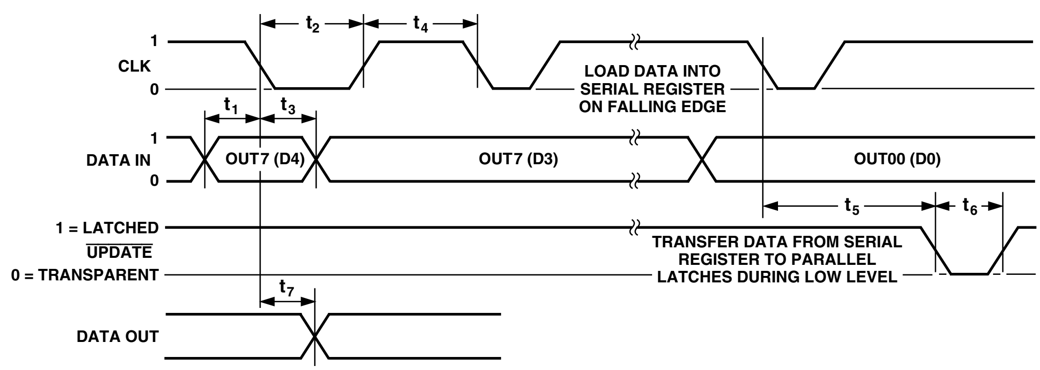


Figure 1. Timing Diagram, Serial Mode

Table I. Logic Levels

V_{IH}	V_{IL}	V_{OH}	V_{OL}	I_{IH}	I_{IL}	I_{OH}	I_{OL}
$\overline{\text{RESET}}$, $\overline{\text{SER}}$/PAR CLK, DATA IN, $\overline{\text{CE}}$, $\overline{\text{UPDATE}}$	$\overline{\text{RESET}}$, $\overline{\text{SER}}$/PAR CLK, DATA IN, $\overline{\text{CE}}$, $\overline{\text{UPDATE}}$	DATA OUT	DATA OUT	$\overline{\text{RESET}}$, $\overline{\text{SER}}$/PAR CLK, DATA IN, $\overline{\text{CE}}$, $\overline{\text{UPDATE}}$	$\overline{\text{RESET}}$, $\overline{\text{SER}}$/PAR CLK, DATA IN, $\overline{\text{CE}}$, $\overline{\text{UPDATE}}$	DATA OUT	DATA OUT
2.0 V min	0.8 V max	2.7 V min	0.5 V max	20 µA max	–400 µA min	–400 µA max	3.0 mA min

TIMING CHARACTERISTICS (Parallel)

Parameter	Symbol	Limit Min	Limit Max	Unit
Data Setup Time	t_1	20		ns
CLK Pulsewidth	t_2	100		ns
Data Hold Time	t_3	20		ns
CLK Pulse Separation	t_4	100		ns
CLK to $\overline{\text{UPDATE}}$ Delay	t_5	0		ns
$\overline{\text{UPDATE}}$ Pulsewidth	t_6	50		ns
Propagation Delay, $\overline{\text{UPDATE}}$ to Switch On or Off			50	ns
CLK, $\overline{\text{UPDATE}}$ Rise and Fall Times			100	ns
$\overline{\text{RESET}}$ Time			200	ns

Specifications subject to change without notice.

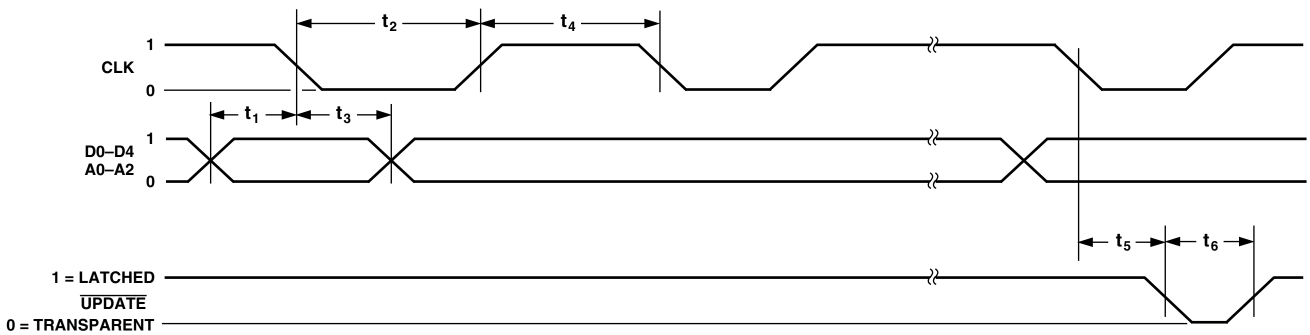


Figure 2. Timing Diagram, Parallel Mode

Table II. Logic Levels

V_{IH}	V_{IL}	V_{OH}	V_{OL}	I_{IH}	I_{IL}	I_{OH}	I_{OL}
$\overline{\text{RESET}}$, $\overline{\text{SER}}$/PAR CLK, D0, D1, D2, D3, D4, A0, A1, A2, A3 $\overline{\text{CE}}$, $\overline{\text{UPDATE}}$	$\overline{\text{RESET}}$, $\overline{\text{SER}}$/PAR CLK, D0, D1, D2, D3, D4, A0, A1, A2, A3 $\overline{\text{CE}}$, $\overline{\text{UPDATE}}$	DATA OUT	DATA OUT	$\overline{\text{RESET}}$, $\overline{\text{SER}}$/PAR CLK, D0, D1, D2, D3, D4, A0, A1, A2, A3 $\overline{\text{CE}}$, $\overline{\text{UPDATE}}$	$\overline{\text{RESET}}$, $\overline{\text{SER}}$/PAR CLK, D0, D1, D2, D3, D4, A0, A1, A2, A3 $\overline{\text{CE}}$, $\overline{\text{UPDATE}}$	DATA OUT	DATA OUT
2.0 V min	0.8 V max	2.7 V min	0.5 V max	20 µA max	–400 µA min	–400 µA max	3.0 mA min

ABSOLUTE MAXIMUM RATINGS[1]

Analog Supply Voltage ($AV_{CC} – AV_{EE}$) . . . . 26.0 V
Digital Supply Voltage (DV_{CC} – DGND) . . . . 6 V
Ground Potential Difference (AGND – DGND) . . . . . ±0.5 V
Internal Power Dissipation[2] . . . . 3.1 W
Analog Input Voltage[3] . . . . Maintain Linear Output
Digital Input Voltage . . . . DV_{CC}
Output Voltage (Disabled Output)
. . . . (AV_{CC} – 1.5 V) to (AV_{EE} + 1.5 V)
Output Short-Circuit Duration . . . . Momentary
Storage Temperature Range . . . . –65°C to +125°C
Lead Temperature Range (Soldering 10 sec) . . . . 300°C

NOTES
[1]Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only; functional operation of the device at these or any other conditions above those indicated in the operational section of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.
[2]Specification is for device in free air (T_A = 25°C):
100-lead plastic LQFP (ST): θ_{JA} = 40°C/W.
[3]To avoid differential input breakdown, in no case should one-half the output voltage (1/2 V_{OUT}) and any input voltage be greater than 10 V potential differential. See output voltage swing specification for linear output range.

POWER DISSIPATION

The AD8113 is operated with ±5 V to ±12 V supplies and can drive loads down to 150 Ω (±5 V) or 600 Ω (±12 V), resulting in a large range of possible power dissipations. For this reason, extra care must be taken derating the operating conditions based on ambient temperature.

Packaged in a 100-lead LQFP, the AD8113 junction-to-ambient thermal impedance (θ_{JA}) is 40°C/W. For long-term reliability, the maximum allowed junction temperature of the plastic-encapsulated die should not exceed 150°C. Temporarily exceeding this limit may cause a shift in parametric performance due to a change in the stresses exerted on the die by the package. Exceeding a junction temperature of 175°C for an extended period can result in device failure. The following curve shows the range of allowed power dissipations that meet these conditions over the commercial range of ambient temperatures.

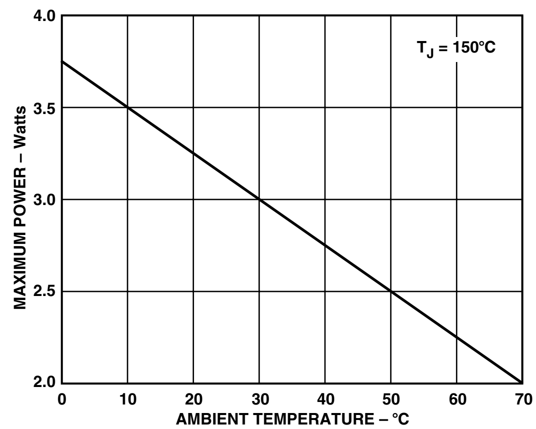


Figure 3. Maximum Power Dissipation vs. Ambient Temperature

ORDERING GUIDE

Model	Temperature Range	Package Description	Package Option
AD8113JST	0°C to 70°C	100-Lead Plastic LQFP (14 mm × 14 mm)	ST-100
AD8113-EVAL		Evaluation Board	

CAUTION

ESD (electrostatic discharge) sensitive device. Electrostatic charges as high as 4000 V readily accumulate on the human body and test equipment and can discharge without detection. Although the AD8113 features proprietary ESD protection circuitry, permanent damage may occur on devices subjected to high energy electrostatic discharges. Therefore, proper ESD precautions are recommended to avoid performance degradation or loss of functionality.

Table III. Operation Truth Table

$\overline{CE}$	$\overline{UPDATE}$	CLK	DATA IN	DATA OUT	$\overline{RESET}$	$\overline{SER}$/PAR	Operation/Comment
1	X	X	X	X	X	X	No change in logic.
0	1	↓	Data $_i$	Data $_{i-80}$	1	0	The data on the serial DATA IN line is loaded into serial register. The first bit clocked into the serial register appears at DATA OUT 80 clocks later.
0	1	↓	D0 . . . D4, A0 . . . A3	NA in Parallel Mode	1	1	The data on the parallel data lines, D0–D4, are loaded into the 80-bit serial shift register location addressed by A0–A3.
0	0	X	X	X	1	X	Data in the 80-bit shift register transfers into the parallel latches that control the switch array. Latches are transparent.
X	X	X	X	X	0	X	Asynchronous operation. All outputs are disabled. Remainder of logic is unchanged.

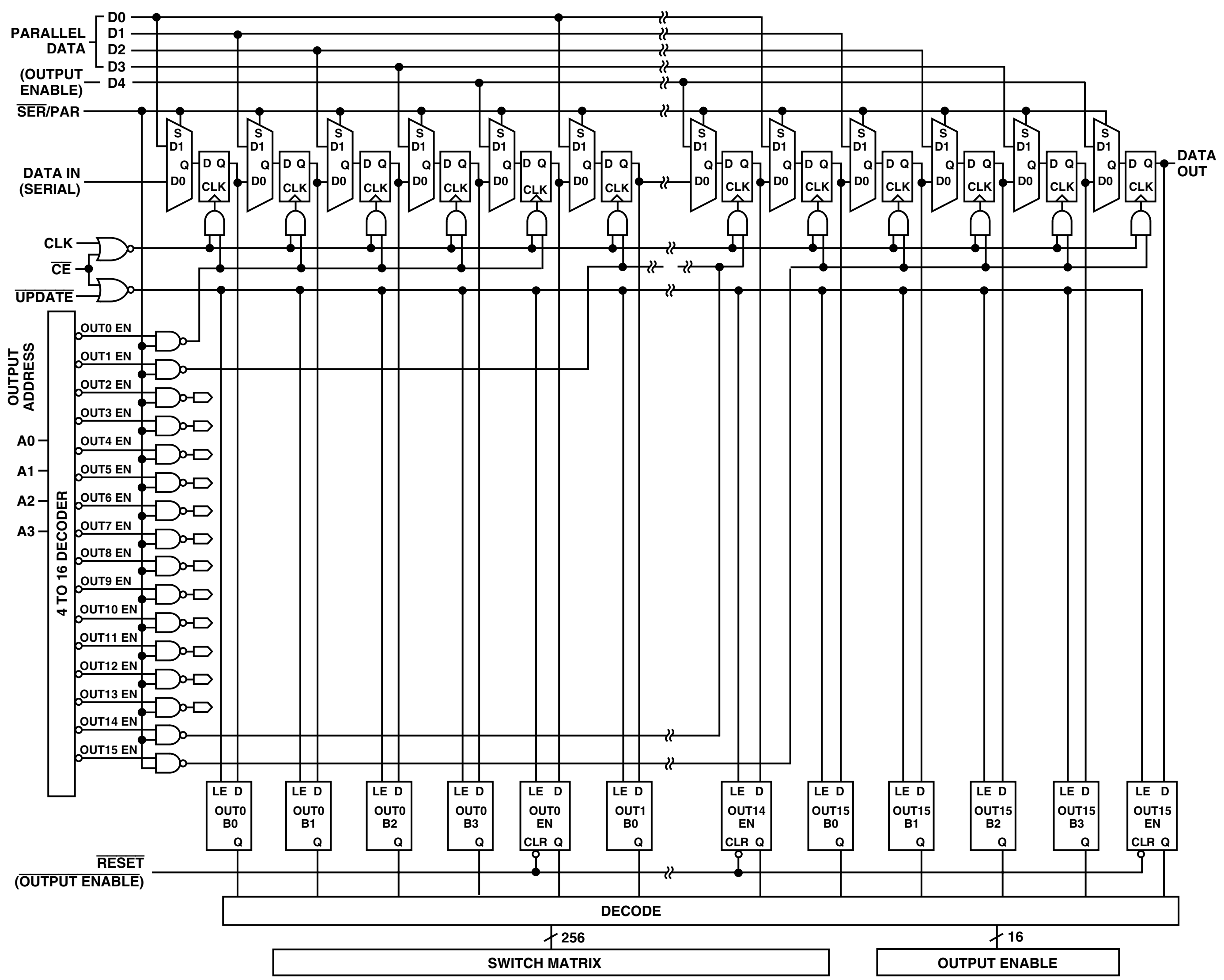
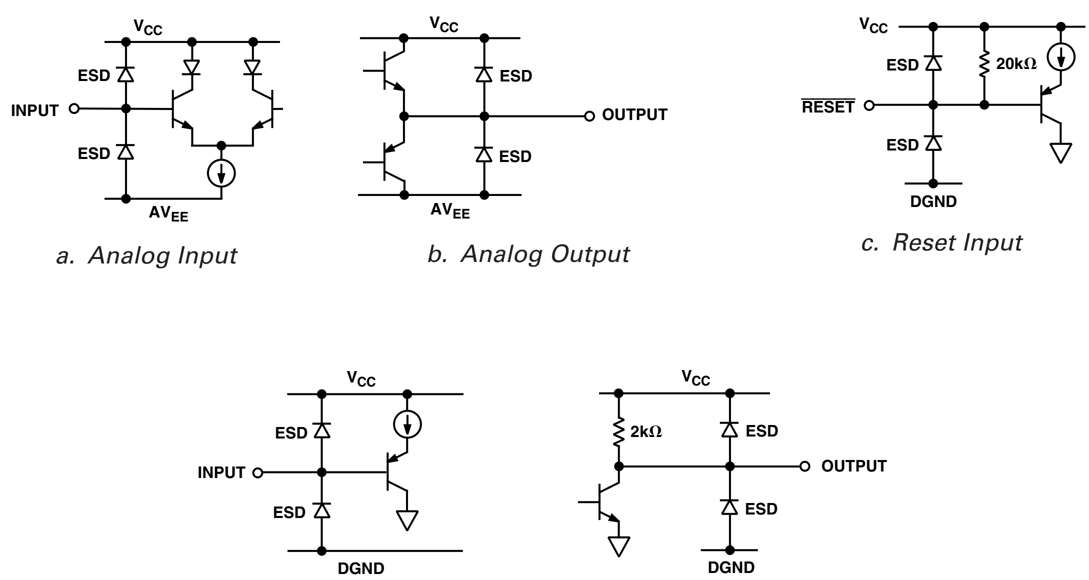


Figure 4. Logic Diagram

PIN FUNCTION DESCRIPTIONS

Mnemonic	Pin Numbers	Pin Description
INxx	58, 60, 62, 64, 66, 68, 70, 72, 4, 6, 8, 10, 12, 14, 16, 18	Analog Inputs; xx = Channel Numbers 00 through 15.
DATA IN	96	Serial Data Input, TTL Compatible.
CLK	97	Clock, TTL Compatible. Falling Edge Triggered.
DATA OUT	98	Serial Data Out, TTL Compatible.
$\overline{\text{UPDATE}}$	95	Enable (Transparent) Low. Allows serial register to connect directly to switch matrix. Data latched when High.
$\overline{\text{RESET}}$	100	Disable Outputs, Active Low.
$\overline{\text{CE}}$	99	Chip Enable, Enable Low. *Must be low to clock in and latch data.*
$\overline{\text{SER}}$/PAR	94	Selects Serial Data Mode, Low or Parallel Data Mode, High. *Must be connected.*
OUTyy	53, 51, 49, 47, 45, 43, 41, 39, 37, 35, 33, 31, 29, 27, 25, 23	Analog Outputs yy = Channel Numbers 00 Through 15.
AGND	3, 5, 7, 9, 11, 13, 15, 17, 19, 57, 59, 61, 63, 65, 67, 69, 71, 73	Analog Ground for Inputs and Switch Matrix. *Must be connected.*
DV_{CC}	1, 75	5 V for Digital Circuitry.
DGND	2, 74	Ground for Digital Circuitry.
AV_{EE}	20, 56	–5 V for Inputs and Switch Matrix.
AV_{CC}	21, 55	5 V for Inputs and Switch Matrix.
AV_{CC}xx/yy	54, 50, 46, 42, 38, 34, 30, 26, 22	5 V for Output Amplifier that is shared by Channel Numbers xx and yy. *Must be connected.*
AV_{EE}xx/yy	52, 48, 44, 40, 36, 32, 28, 24	–5 V for Output Amplifier that is shared by Channel Numbers xx and yy. *Must be connected.*
A0	84	Parallel Data Input, TTL Compatible (Output Select LSB).
A1	83	Parallel Data Input, TTL Compatible (Output Select).
A2	82	Parallel Data Input, TTL Compatible (Output Select).
A3	81	Parallel Data Input, TTL Compatible (Output Select MSB).
D0	80	Parallel Data Input, TTL Compatible (Input Select LSB).
D1	79	Parallel Data Input, TTL Compatible (Input Select).
D2	78	Parallel Data Input, TTL Compatible (Input Select).
D3	77	Parallel Data Input, TTL Compatible (Input Select MSB).
D4	76	Parallel Data Input, TTL Compatible (Output Enable).
NC	85–93	No Connect.



a. Analog Input

b. Analog Output

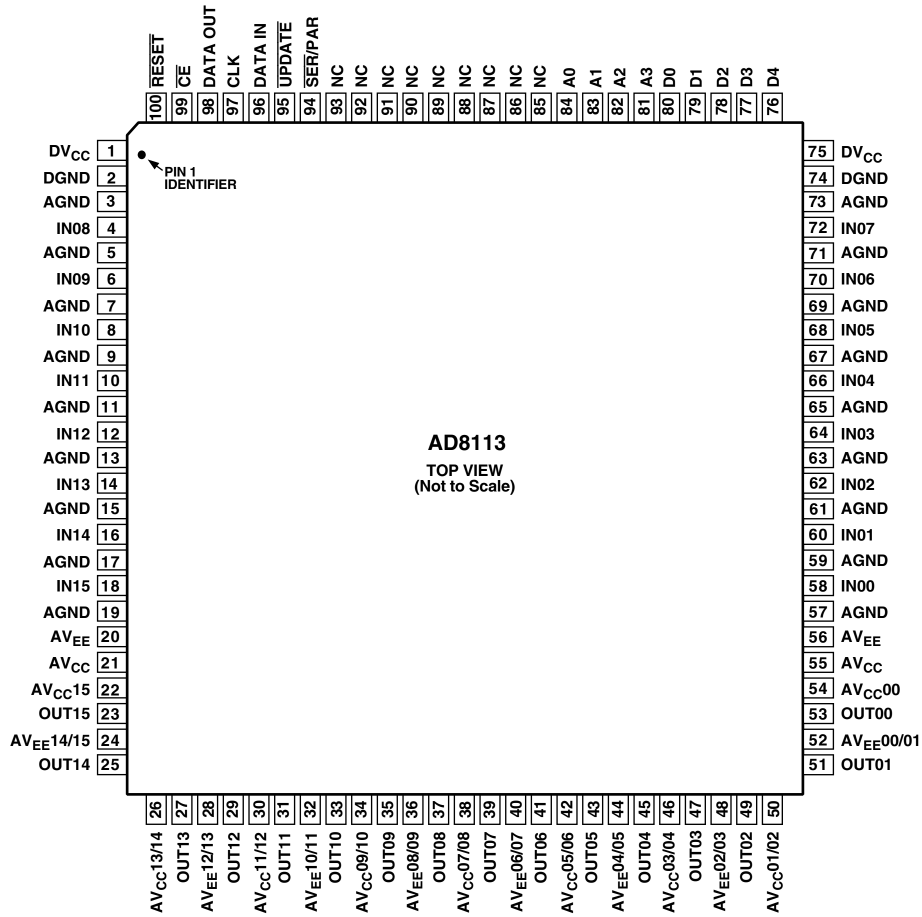
c. Reset Input

d. Logic Input

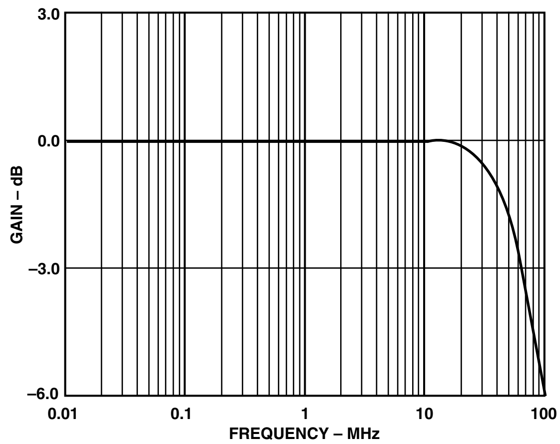
e. Logic Output

Figure 5. I/O Schematics

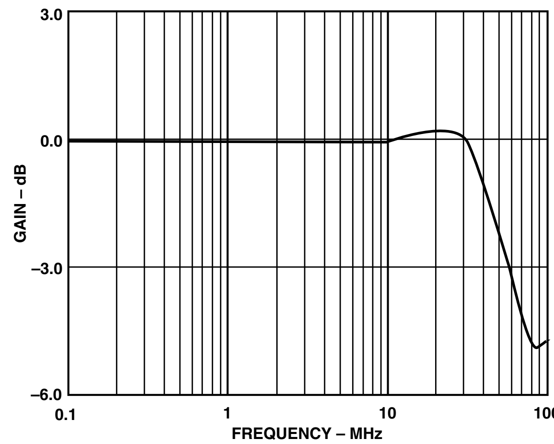
PIN CONFIGURATION



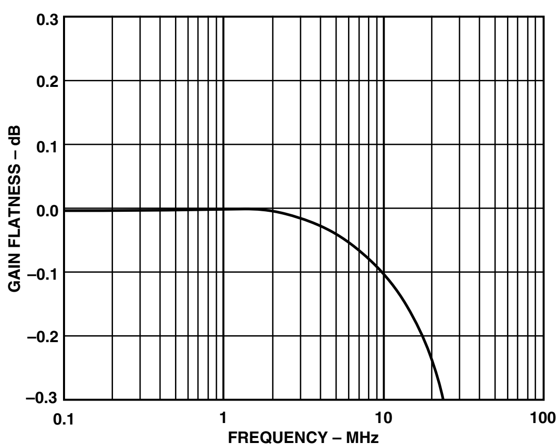
NC = NO CONNECT



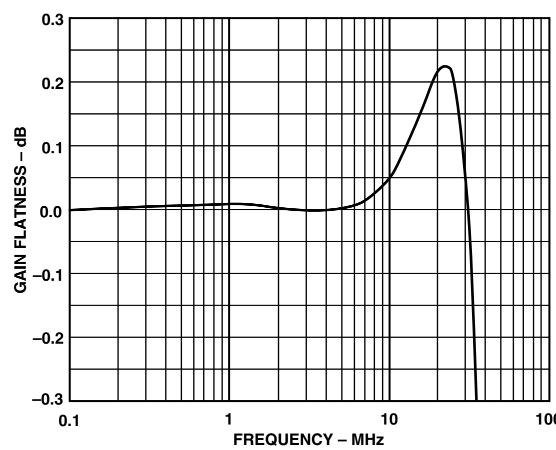
TPC 1. Small Signal Bandwidth, $V_S = \pm 5$ V, $R_L = 150\ \Omega$, $V_{OUT} = 200$ mV p-p



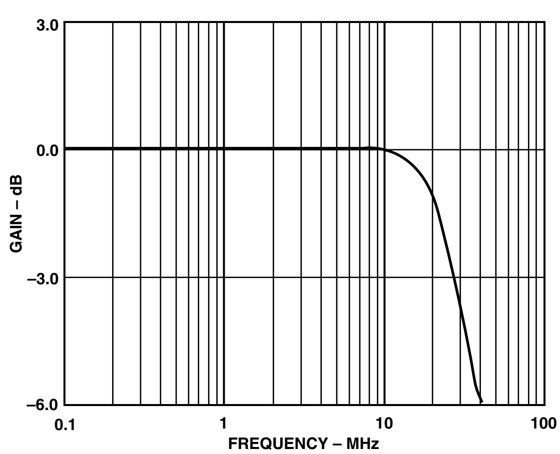
TPC 4. Small Signal Bandwidth, $V_S = \pm 12$ V, $R_L = 600\ \Omega$, $V_{OUT} = 200$ mV p-p



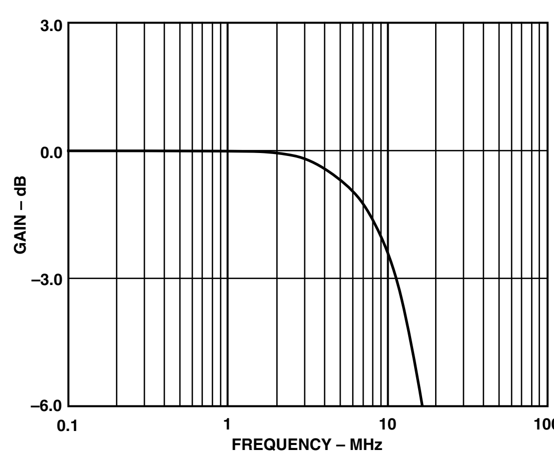
TPC 2. Small Signal Gain Flatness, $V_S = \pm 5$ V, $R_L = 150\ \Omega$, $V_{OUT} = 200$ mV p-p



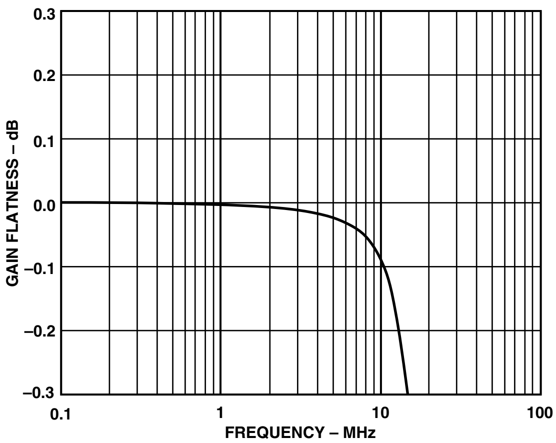
TPC 5. Small Signal Gain Flatness, $V_S = \pm 12$ V, $R_L = 600\ \Omega$, $V_{OUT} = 200$ mV p-p



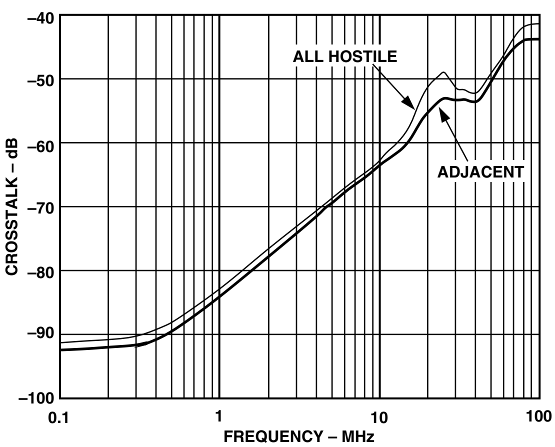
TPC 3. Large Signal Bandwidth, $V_S = \pm 5$ V, $R_L = 150\ \Omega$, $V_{OUT} = 2$ V p-p



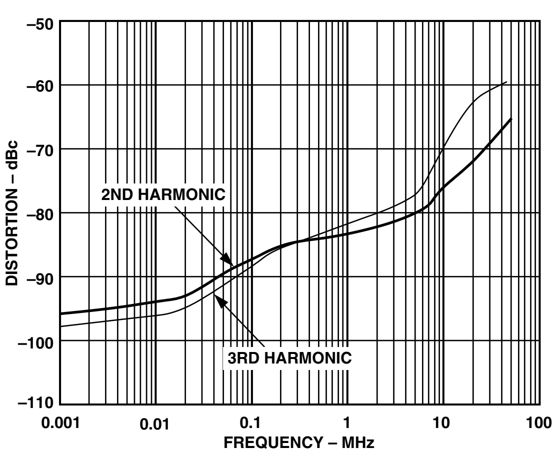
TPC 6. Large Signal Bandwidth, $V_S = \pm 12$ V, $R_L = 600\ \Omega$, $V_{OUT} = 8$ V p-p



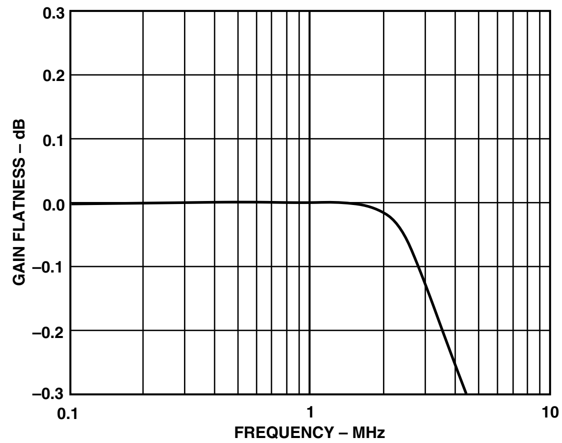
TPC 7. Large Signal Gain Flatness, $V_S = \pm 5$ V, $R_L = 150\ \Omega$, $V_{OUT} = 2$ V p-p



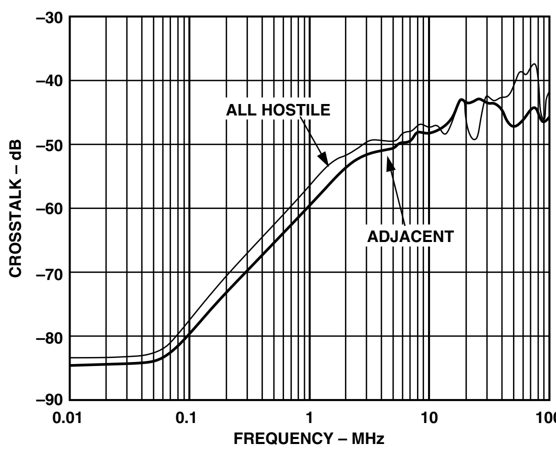
TPC 8. Crosstalk vs. Frequency, $V_S = \pm 5$ V, $R_L = 150\ \Omega$, $V_{OUT} = 2$ V p-p



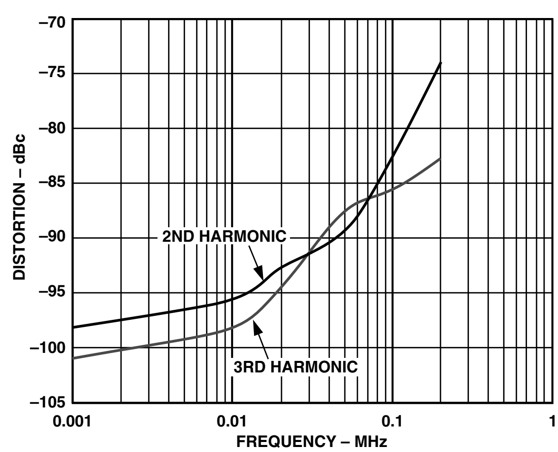
TPC 9. Distortion vs. Frequency, $V_S = \pm 5$ V, $R_L = 150\ \Omega$, $V_{OUT} = 2$ V p-p



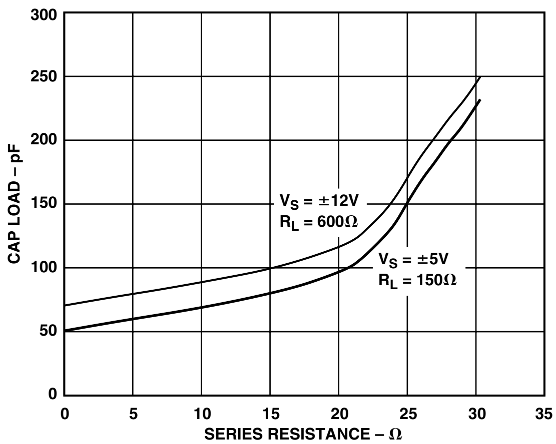
TPC 10. Large Signal Gain Flatness, $V_S = \pm 12$ V, $R_L = 600\ \Omega$, $V_{OUT} = 8$ V p-p



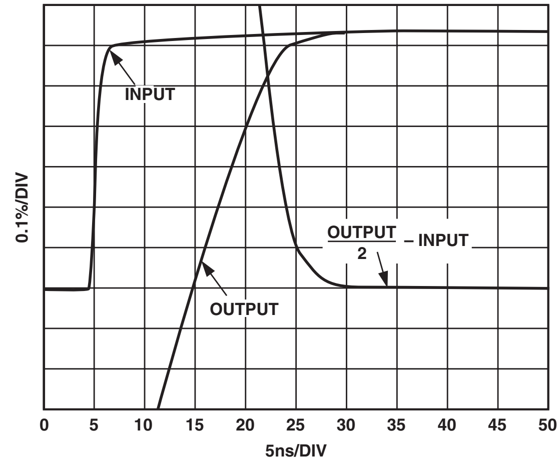
TPC 11. Crosstalk vs. Frequency, $V_S = \pm 12$ V, $R_L = 600\ \Omega$, $V_{OUT} = 20$ V p-p



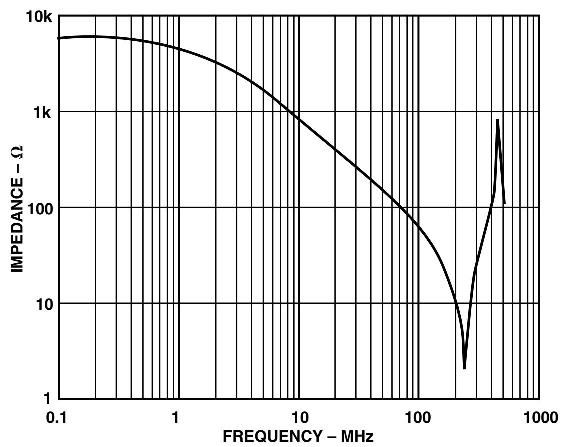
TPC 12. Distortion vs. Frequency, $V_S = \pm 12$ V, $R_L = 600\ \Omega$, $V_{OUT} = 20$ V p-p



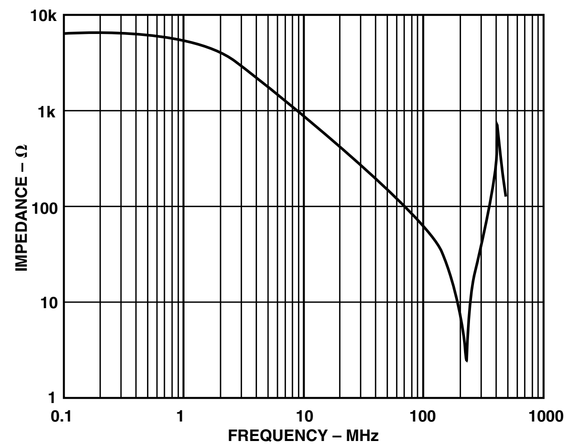
TPC 13. Cap Load vs. Series Resistance for Less than 30% Overshoot



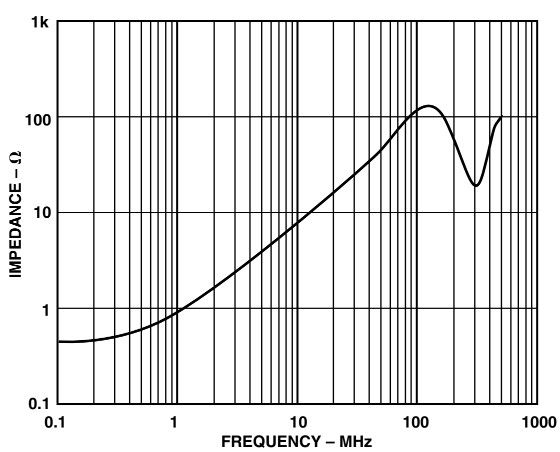
TPC 16. Settling Time to 0.1%, 2 V Step, $V_S = \pm 5$ V, $R_L = 150\ \Omega$



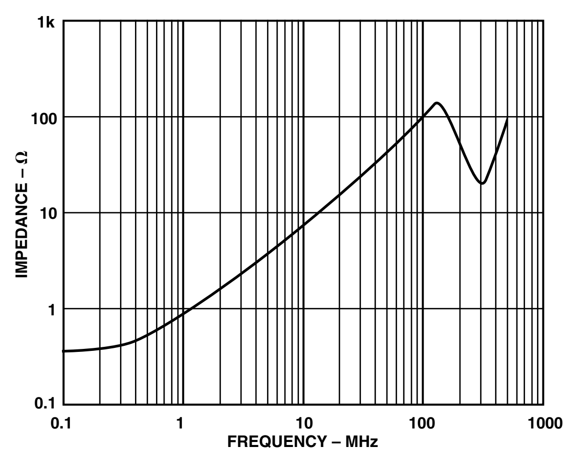
TPC 14. Disabled Output Impedance vs. Frequency, $V_S = \pm 5$ V



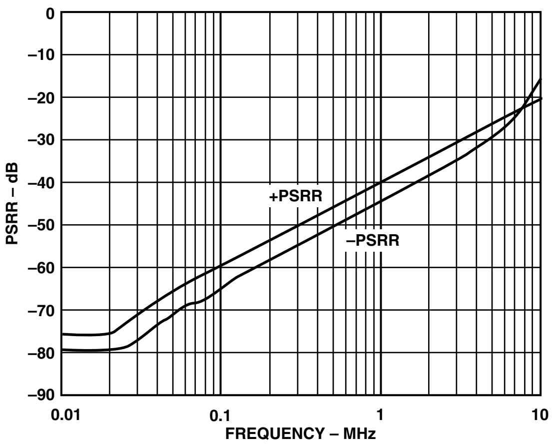
TPC 17. Disabled Output Impedance vs. Frequency, $V_S = \pm 12$ V



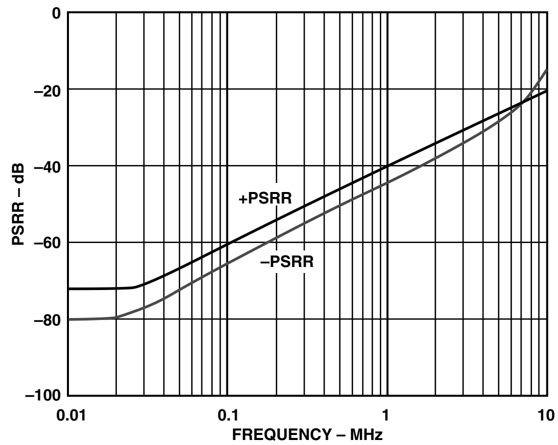
TPC 15. Enabled Output Impedance vs. Frequency, $V_S = \pm 5$ V



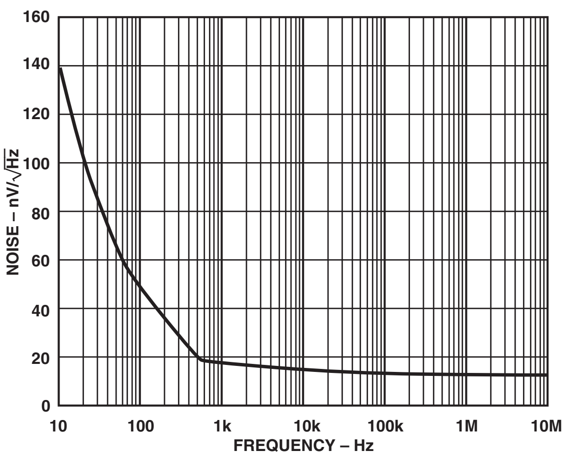
TPC 18. Enabled Output Impedance vs. Frequency, $V_S = \pm 12$ V



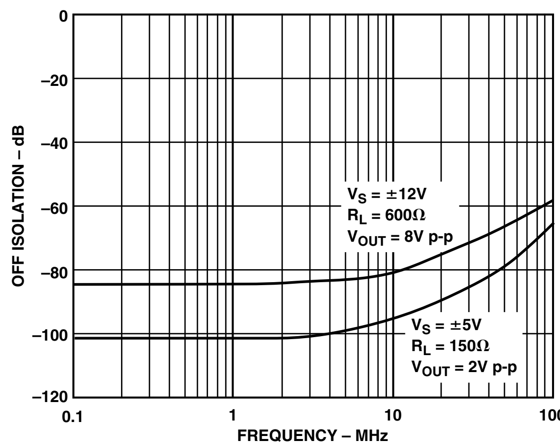
TPC 19. PSRR vs. Frequency, $V_S = \pm 5$ V



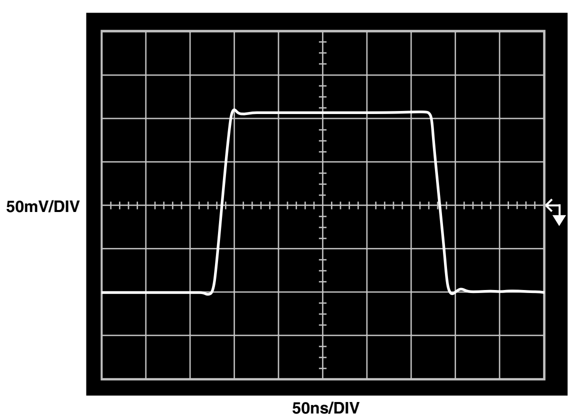
TPC 22. PSRR vs. Frequency, $V_S = \pm 12$ V



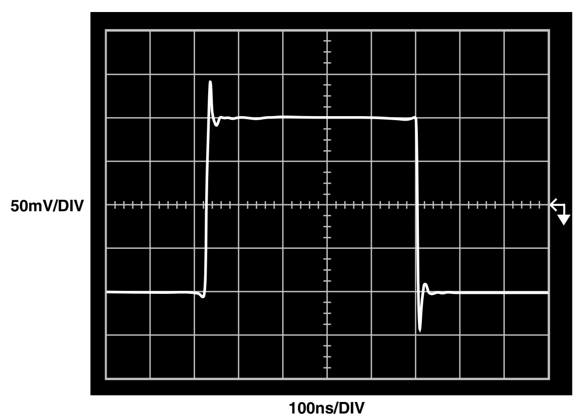
TPC 20. Noise vs. Frequency



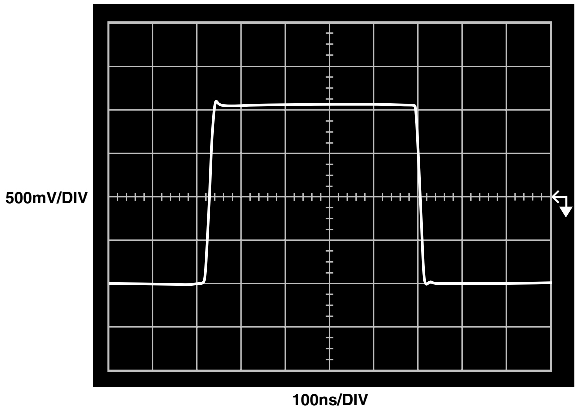
TPC 23. Off Isolation vs. Frequency



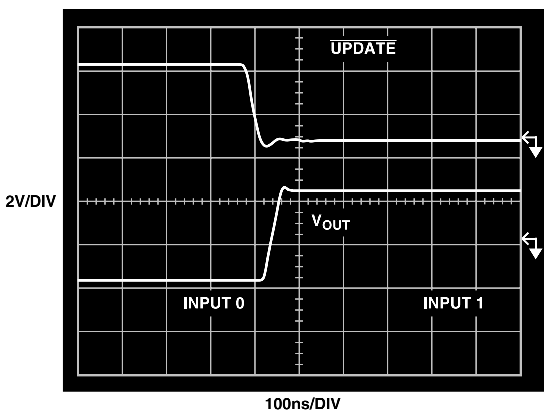
TPC 21. Small Signal Pulse Response, $V_S = \pm 5$ V, $R_L = 150\ \Omega$



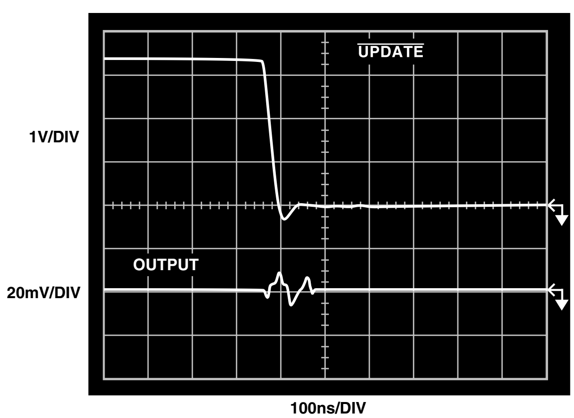
TPC 24. Small Signal Pulse Response, $V_S = \pm 12$ V, $R_L = 600\ \Omega$



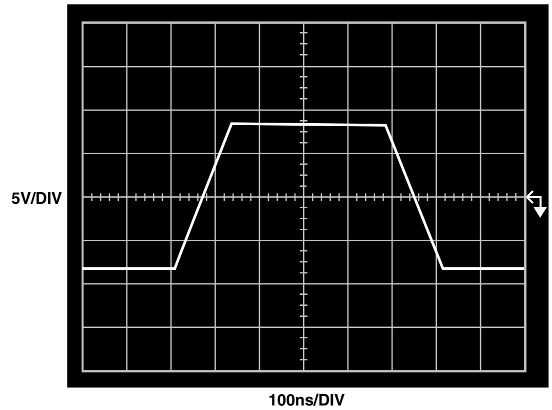
TPC 25. Large Signal Pulse Response, $V_S = \pm 5$ V, $R_L = 150\ \Omega$



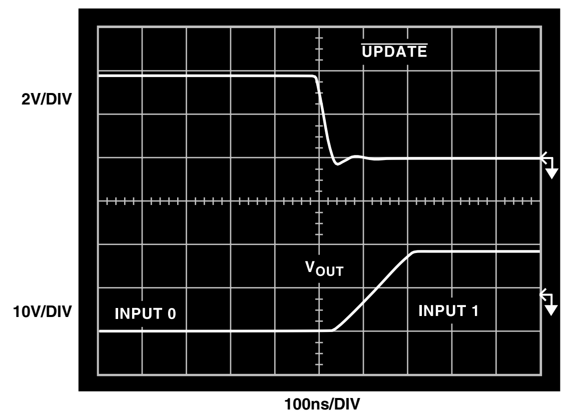
TPC 26. Switching Time, $V_S = \pm 5$ V, $R_L = 150\ \Omega$



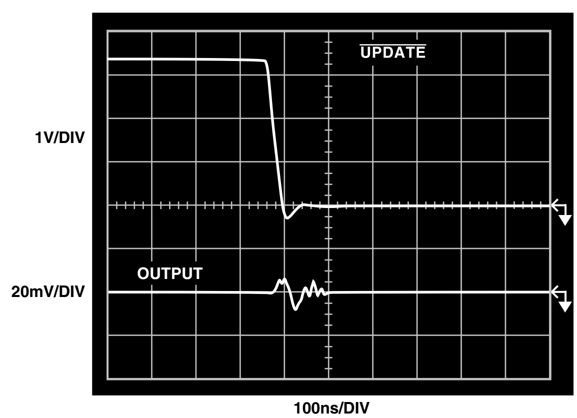
TPC 27. Switching Transient, $V_S = \pm 5$ V, $R_L = 150\ \Omega$



TPC 28. Large Signal Pulse Response, $V_S = \pm 12$ V, $R_L = 600\ \Omega$



TPC 29. Switching Time, $V_S = \pm 12$ V, $R_L = 600\ \Omega$



TPC 30. Switching Transient, $V_S = \pm 12$ V, $R_L = 600\ \Omega$

THEORY OF OPERATION

The AD8113 is a gain-of-two crosspoint array with 16 outputs, each of which can be connected to any one of 16 inputs. Organized by output row, 16 switchable transconductance stages are connected to each output buffer in the form of a 16-to-1 multiplexer. Each of the 16 rows of transconductance stages are wired in parallel to the 16 input pins, for a total array of 256 transconductance stages. Decoding logic for each output selects one (or none) of the transconductance stages to drive the output stage. The transconductance stages are NPN input differential pairs, sourcing current into the folded cascode output stage. The compensation networks and emitter follower output buffers are in the output stage. Voltage feedback sets the gain at +2.

When operated with ±12 V supplies, this architecture provides ±10 V drive for 600 Ω audio loads with extremely low distortion (<0.002%) at audio frequencies. Provided the supplies are lowered to ±5 V (to limit power consumption), the AD8113 can drive reverse-terminated video loads, swinging ±3.0 V into 150 Ω. Disabling unused outputs and transconductance stages minimizes on-chip power consumption.

Features of the AD8113 facilitate the construction of larger switch matrices. The unused outputs can be disabled, leaving only a feedback network resistance of 4 kΩ on the output. This allows multiple ICs to be bused together, provided the output load impedance is greater than minimum allowed values. Because no additional input buffering is necessary, high input resistance and low input capacitance are easily achieved without additional signal degradation.

The AD8113 inputs have a unique bias current compensation scheme that overcomes a problem common to transconductance input array architectures. Typically, input bias current increases as more and more transconductance stages connected to the same input are turned on. Anywhere from zero to 16 transconductance stages can be sharing one input pin, so there is a varying amount of bias current supplied through the source impedance driving the input. For audio systems with larger source impedances, this has the potential of creating large offset voltages, audible as pops when switching between channels. The AD8113 samples and cancels the input bias current contributions from each transconductance stage so that the residual bias current is nominally zero regardless of the number of enabled inputs.

Due to the flexibility in allowed supply voltages, internal crosstalk isolation clamps have variable bias levels. These levels were chosen to allow for the necessary input range to accommodate the full output swing with a gain of two. Overdriving the inputs beyond the device’s linear range will eventually forward bias these clamps, increasing power dissipation. The valid input range for ±12 V supplies is ±5 V. The valid input range for ±5 V supplies is ±1.5 V. When outputs are disabled and being driven externally, the voltage applied to them should not exceed the valid output swing range for the AD8113. Exceeding ±10.5 V on the outputs of the AD8113 may apply a large differential voltage on the unused transconductance stages and should be avoided.

A flexible TTL compatible logic interface simplifies the programming of the matrix. Either parallel or serial loading into a first rank of latches programs each output. A global latch simultaneously updates all outputs. In serial mode, a serial-out pin allows devices to be daisy chained together for single pin programming of multiple ICs. A power-on reset pin is available to avoid bus conflicts by disabling all outputs.

Regardless of the supply voltage applied to the AV_{CC} and AV_{EE} pins, the digital logic requires 5 V on the DV_{CC} pin with respect to DGND. In order for the digital-to-analog interface to work properly, DV_{CC} must be at least 7 V above AV_{EE}. Finally, internal ESD protection diodes require that the DGND and AGND pins be at the same potential.

CALCULATION OF POWER DISSIPATION

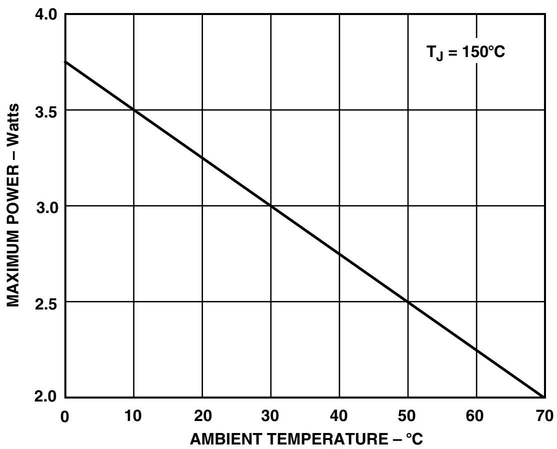


Figure 6. Maximum Power Dissipation vs. Ambient Temperature

The above curve was calculated from

$$P_{D,\,MAX} = \frac{\left(T_{JUNCTION,\,MAX} - T_{AMBIENT}\right)}{\theta_{JA}}$$

As an example, if the AD8113 is enclosed in an environment at 50°C (T_A), the total on-chip dissipation under all load and supply conditions must not be allowed to exceed 2.5 W.

When calculating on-chip power dissipation, it is necessary to include the rms current being delivered to the load, multiplied by the rms voltage drop on the AD8113 output devices. The dissipation of the on-chip, 4 kΩ feedback resistor network must also be included. For a sinusoidal output, the on-chip power dissipation due to the load and feedback network can be approximated by

$$P_{D,\,MAX} = \left(AV_{CC} - V_{OUTPUT,\,RMS}\right) \times I_{OUTPUT,\,RMS} + \left(\frac{V_{OUTPUT,\,RMS}^{\;2}}{4\ k\Omega}\right)$$

For nonsinusoidal output, the power dissipation should be calculated by integrating the on-chip voltage drop multiplied by the load current over one period.

The user may subtract the quiescent current for the Class AB output stage when calculating the loaded power dissipation. For each output stage driving a load, subtract a quiescent power according to

$$P_{D,\,OUTPUT} = \left(AV_{CC} - AV_{EE}\right) \times I_{O,\,QUIESCENT}$$

For the AD8113, $I_{O,\,QUIESCENT}$ = 0.67 mA.

For each disabled output, the quiescent power supply current in AV_{CC} and AV_{EE} drops by approximately 1.25 mA, although there is a power dissipation in the on-chip feedback resistors if the disabled output is being driven from an external source.

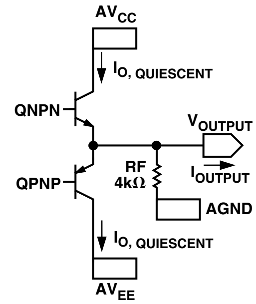


Figure 7. Simplified Output Stage

An example: AD8113, in an ambient temperature of 70°C, with all 16 outputs driving 6 V rms into 600 Ω loads. Power supplies are ±12 V.

Step 1. Calculate power dissipation of AD8113 using data sheet quiescent currents.

$$P_{D,\,QUIESCENT} = (AV_{CC} \times I_{AVCC}) + (AV_{EE} \times I_{AVEE}) + (DV_{CC} \times I_{DVCC})$$

$$P_{D,\,QUIESCENT} = (12\ V \times 54\ mA) + (-12\ V \times -54\ mA) + (5\ V \times 13\ mA)$$

Step 2. Calculate power dissipation from loads.

$$P_{D,\,OUTPUT} = (AV_{CC} - V_{OUTPUT,\,RMS}) \times I_{OUTPUT,\,RMS} + V_{OUTPUT}^{2}/4\ k\Omega$$

$$P_{D,\,OUTPUT} = (12\ V - 6\ V) \times 6\ V/600\ \Omega + (6\ V)^2/4\ k\Omega = 69\ mW$$

There are 16 outputs, so

$$nP_{D,\,OUTPUT} = 16 \times 69\ mW = 1.1\ W$$

Step 3. Subtract quiescent output current for number of loads (assumes output voltage >> 0.5 V).

$$P_{DQ,\,OUTPUT} = (AV_{CC} - AV_{EE}) \times I_{O,\,QUIESCENT}$$

$$P_{DQ,\,OUTPUT} = (12\ V - (-12\ V)) \times 0.67\ mA = 16\ mW$$

There are 16 outputs, so

$$nP_{D,\,OUTPUT} = 16 \times 16\ mW = 0.3\ W$$

Step 4. Verify that power dissipation does not exceed maximum allowed value.

$$P_{D,\,ON\text{-}CHIP} = P_{D,\,QUIESCENT} + nP_{D,\,OUTPUT} - nP_{DQ,\,OUTPUT}$$

$$P_{D,\,ON\text{-}CHIP} = 1.3\ W + 1.1\ W - 0.3\ W = 2.1\ W$$

From the figure or the equation, this power dissipation is below the maximum allowed dissipation for all ambient temperatures approaching 70°C.

NOTE: It can be shown that for a dual supply of ±*a*, a Class AB output stage dissipates maximum power into a grounded load when the output voltage is *a*/2. So for a ±12 V supply, the above example demonstrates the worst-case power dissipation into 600 Ω. It can be seen from this example that the minimum load resistance for ±12 V operation is 600 Ω (for full rated operating temperature range). For larger safety margins, when the output signal is unknown, loads of 1 kΩ and greater are recommended. When operating with ±5 V supplies, this load resistance may be lowered to 150 Ω.