50 dB GSM PA Controller

AD8315

FEATURES

Complete RF Detector/Controller Function
>50 dB Range at 0.9 GHz (–49 dBm to +2 dBm re 50 Ω)
Accurate Scaling from 0.1 GHz to 2.5 GHz
Temperature-Stable Linear-in-dB Response
Log Slope of 23 mV/dB, Intercept at –60 dBm at 0.9 GHz
True Integration Function in Control Loop
Low Power: 20 mW at 2.7 V, 38 mW at 5 V
Power Down to 10.8 μW

APPLICATIONS

Single, Dual, and Triple Band Mobile Handset (GSM, DCS, EDGE)
Transmitter Power Control

PRODUCT DESCRIPTION

The AD8315 is a complete low cost subsystem for the precise control of RF power amplifiers operating in the frequency range 0.1 GHz–2.5 GHz and over a typical dynamic range of 50 dB. It is intended for use in cellular handsets and other battery-operated wireless devices. The log amp technique provides a much wider measurement range and better accuracy than controllers using diode detectors. In particular, its temperature stability is excellent over a specified range of –30°C to +85°C.

Its high sensitivity allows control at low signal levels, thus reducing the amount of power that needs to be coupled to the detector.

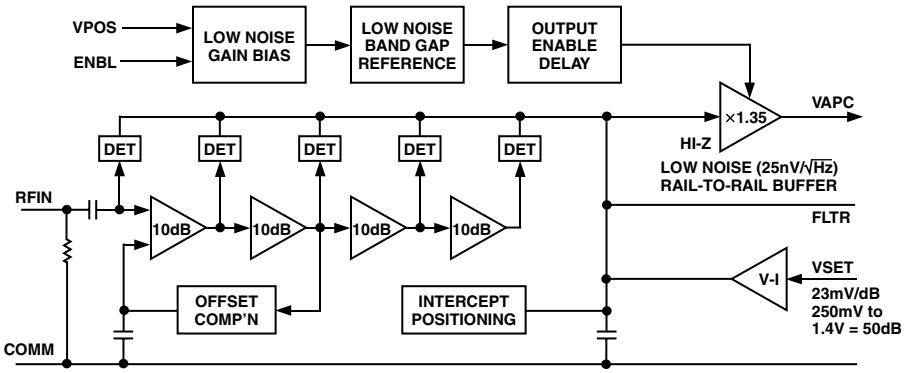
For convenience, the signal is internally ac-coupled. This high-pass coupling, with a corner at approximately 0.016 GHz, determines the lowest operating frequency. Thus, the source may be dc grounded.

The AD8315 provides a voltage output, VAPC, that has the voltage range and current drive to directly connect to most handset power amplifiers' gain control pin. VAPC can swing from 250 mV above ground to within 200 mV below the supply voltage. Load currents of up to 6 mA can be supported.

The setpoint control input is applied to pin VSET and has an operating range of 0.25 V–1.4 V. The associated circuit determines the slope and intercept of the linear-in-dB measurement system; these are nominally 23 mV/dB and –60 dBm for a 50 Ω termination (–73 dBV) at 0.9 GHz. Further simplifying the application of the AD8315, the input resistance of the setpoint interface is over 100 MΩ, and the bias current is typically 0.5 μA.

The AD8315 is available in MSOP and lead frame chip scale (LFCSP) packages and consumes 8.5 mA from a 2.7 V to 5.5 V supply. When powered down, the sleep current is 4 μA.

FUNCTIONAL BLOCK DIAGRAM



REV. B

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AD8315—SPECIFICATIONS (V_S = 2.7 V, T = 25°C, 52.3 Ω termination on RFIN, unless otherwise noted.)

Parameter	Conditions	Min	Typ	Max	Unit
OVERALL FUNCTION					
Frequency Range[1]	To Meet All Specifications	0.1		2.5	GHz
Input Voltage Range	±1 dB Log Conformance, 0.1 GHz	–57		–11	dBV
Equivalent dBm Range		–44		+2	dBm
Logarithmic Slope[2]	0.1 GHz	21.5	24	25.5	mV/dB
Logarithmic Intercept[2]	0.1 GHz	–79	–70	–64	dBV
Equivalent dBm Level		–66	–57	–51	dBm
RF INPUT INTERFACE	Pin RFIN				
Input Resistance[3]	0.1 GHz		2.8		kΩ
Input Capacitance[3]	0.1 GHz		0.9		pF
OUTPUT	Pin VAPC				
Minimum Output Voltage	VSET ≤ 200 mV, ENBL High	0.25	0.27	0.3	V
	ENBL Low		0.02		V
Maximum Output Voltage	$R_L \geq 800\ \Omega$	2.45		2.6	V
vs. Temperature[4]	85°C, V_{POS} = 3 V, I_{OUT} = 6 mA	2.54			V
General Limit	2.7 V ≤ VPOS ≤ 5.5 V, $R_L = \infty$		VPOS – 0.1		V
Output Current Drive	Source/Sink		5/200		mA/μA
Output Buffer Noise			25		$nV\sqrt{Hz}$
Output Noise	RF Input = 2 GHz, 0 dBm, f_{NOISE} = 100 kHz, C_{FLT} = 220 pF		130		$nV/\sqrt{Hz}$
Small Signal Bandwidth	0.2 V to 2.6 V Swing		30		MHz
Slew Rate	10%–90%, 1.2 V Step (V_{SET}), Open Loop[5]		13		V/μs
Response Time	FLTR = Open, Refer to TPC 24		150		ns
SETPOINT INTERFACE	Pin VSET				
Nominal Input Range	Corresponding to Central 50 dB	0.25		1.4	V
Logarithmic Scale Factor			43.5		dB/V
Input Resistance			100		kΩ
Slew Rate			16		V/μs
ENABLE INTERFACE	Pin ENBL				
Logic Level to Enable Power		1.8		V_{POS}	V
Input Current when Enable High			20		μA
Logic Level to Disable Power				0.8	V
Enable Time	Time from ENBL High to V_{APC} within 1% of Final Value, V_{SET} ≤ 200 mV, Refer to TPC 21		4	5	μs
Disable Time	Time from ENBL Low to V_{APC} within 1% of Final Value, V_{SET} ≤ 200 mV, Refer to TPC 21		8	9	μs
Power-On/Enable Time	Time from VPOS/ENBL High to V_{APC} within 1% of Final Value, V_{SET} ≤ 200 mV, Refer to TPC 26		2	3	μs
	Time from VPOS/ENBL Low to V_{APC} within 1% of Final Value, V_{SET} ≤ 200 mV, Refer to TPC 26		100	200	ns
POWER INTERFACE	Pin VPOS				
Supply Voltage		2.7		5.5	V
Quiescent Current	ENBL High		8.5	10.7	mA
Over Temperature	–30°C ≤ T_A ≤ +85°C			12.9	mA
Disable Current[6]	ENBL Low		4	10	μA
Over Temperature	–30°C ≤ T_A ≤ +85°C			13	μA

NOTES
[1]Operation down to 0.02 GHz is possible.
[2]Mean and Standard Deviation specifications are available in Table I.
[3]See TPC 9 for plot of Input Impedance vs. Frequency.
[4]This parameter is guaranteed but not tested in production. Limit is –3 sigma from the mean.
[5]Response time in a closed-loop system will depend upon the filter capacitor (C_{FLT}) used and the response of the variable gain element.
[6]This parameter is guaranteed but not tested in production. Maximum specified limit on this parameter is the +6 sigma value.

Specifications subject to change without notice.

Table I. Typical Specifications at Selected Frequencies at 25°C (Mean and Sigma)

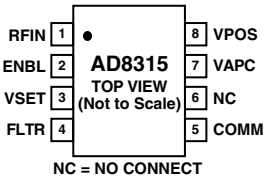
					±1 dB Dynamic Range			
	Slope – mV/dB		Intercept – dBV		Low Point – dBV		High Point – dBV	
Frequency – GHz	Mean	Sigma	Mean	Sigma	Mean	Sigma	Mean	Sigma
0.1	23.8	0.3	–70.1	1.8	–57.7	1.3	–10.6	0.8
0.9	23.2	0.4	–72.6	1.8	–61.0	1.3	–11.2	0.8
1.9	22.2	0.3	–73.8	1.6	–62.9	0.9	–18.5	1.7
2.5	22.3	0.4	–75.6	1.5	–64.0	1.1	–20.0	1.7

ABSOLUTE MAXIMUM RATINGS*

Supply Voltage VPOS . . . . . 5.5 V
Temporary Overvoltage VPOS
(100 cycles, 2 seconds duration, ENBL Low) . . . . . 6.3 V
VAPC, VSET, ENBL . . . . . 0 V, VPOS
RFIN . . . . . 17 dBm
Equivalent Voltage . . . . . 1.6 V rms
Internal Power Dissipation . . . . . 60 mW
θ_{JA} (MSOP) . . . . . 200°C/W
θ_{JA} (LFCSP, Paddle Soldered) . . . . . 80°C/W
θ_{JA} (LFCSP, Paddle not Soldered) . . . . . 200°C/W
Maximum Junction Temperature . . . . . 125°C
Operating Temperature Range . . . . . –40°C to +85°C
Storage Temperature Range . . . . . –65°C to +150°C
Lead Temperature Range (Soldering 60 sec)
MSOP . . . . . 300°C
LFCSP . . . . . 240°C

*Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only; functional operation of the device at these or any other conditions above those indicated in the operational section of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

PIN CONFIGURATION



PIN FUNCTION DESCRIPTIONS

Pin No.	Mnemonic	Function
1	RFIN	RF Input
2	ENBL	Connect to VPOS for Normal Operation Connect pin to ground for Disable Mode
3	VSET	Setpoint Input. Nominal input range 0.25 V to 1.4 V.
4	FLTR	Integrator Capacitor. Connect between FLTR and COMM.
5	COMM	Device Common (Ground)
6	NC	No Connection
7	VAPC	Output. Control voltage for gain control element.
8	VPOS	Positive Supply Voltage: 2.7 V to 5.5 V

ORDERING GUIDE

Model	Temperature Range	Package Descriptions	Package Option	Branding Information
AD8315ARM	–30°C to +85°C	Tube, 8-Lead MSOP	RM-8	J7A
AD8315ARM-REEL		13" Tape and Reel		
AD8315ARM-REEL7		7" Tape and Reel		
AD8315-EVAL		MSOP Evaluation Board		
AD8315ACP-REEL	–30°C to +85°C	13" Tape and Reel, 8-Lead LFCSP	CP-8	J7A
AD8315ACP-REEL7		7" Tape and Reel		
AD8315ACP-EVAL		LFCSP Evaluation Board		

CAUTION

ESD (electrostatic discharge) sensitive device. Electrostatic charges as high as 4000 V readily accumulate on the human body and test equipment and can discharge without detection. Although the AD8315 features proprietary ESD protection circuitry, permanent damage may occur on devices subjected to high energy electrostatic discharges. Therefore, proper ESD precautions are recommended to avoid performance degradation or loss of functionality.

Revision History

Location	Page
1/03—Data Sheet changed from REV. 0 to REV. B.	
Edits to PRODUCT DESCRIPTION section	1
Edit to FUNCTIONAL BLOCK DIAGRAM	1
Edits to SPECIFICATIONS	2
Edits to ABSOLUTE MAXIMUM RATINGS	3
ORDERING GUIDE updated	3
TPC 9 replaced with new figure	5
Edits to TPC 27	8
Edit to Figure 1	9
Edit to Figure 3	10
Edit to Equation 9	10
Edit to Equation 10	10
Edit to Equation 11	10
Edits to Example section	10
Edit to Basic Connections section	12
Edits to Input Coupling Options section	14
Table III becomes Table II	15
Table II Recommended Components deleted	15
Using the Chip-Scale Package section added	15
Edits to Evaluation Board section	15
Figure 12 title edited	16
Figure 13 title edited	16
8-Lead Chip Scale Package (CP-8) added	17
Updated OUTLINE DIMENSIONS	17

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